Lucerne University of
Applied Sciences and Arts

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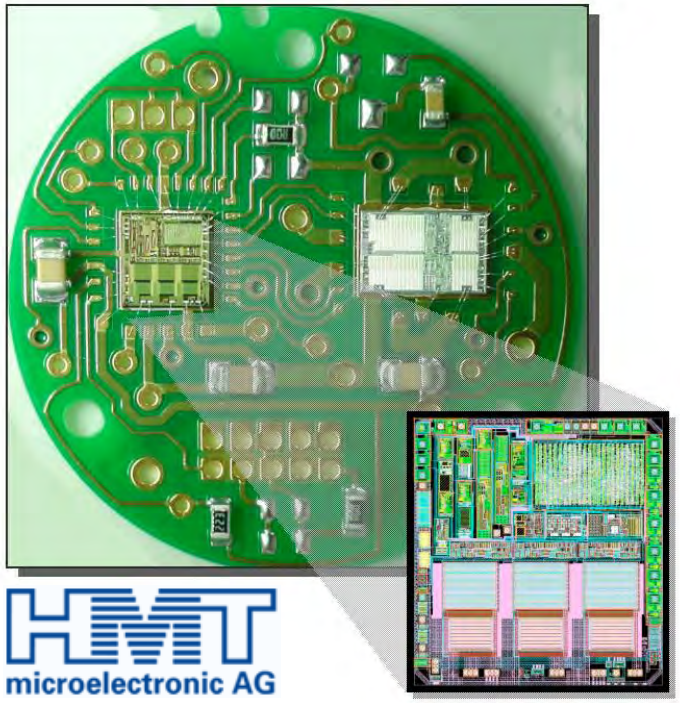
COMSOL
CONFERENCE
STUTTGART 2011
OCTOBER 26-28

Heat Removal of a Protection Chip after Surge Pulse



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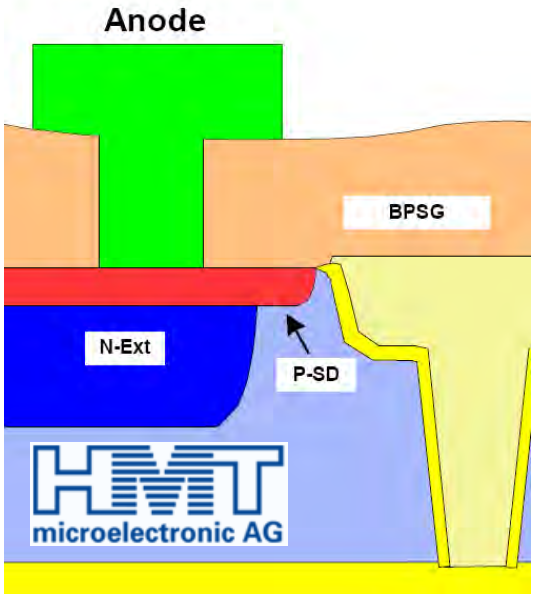
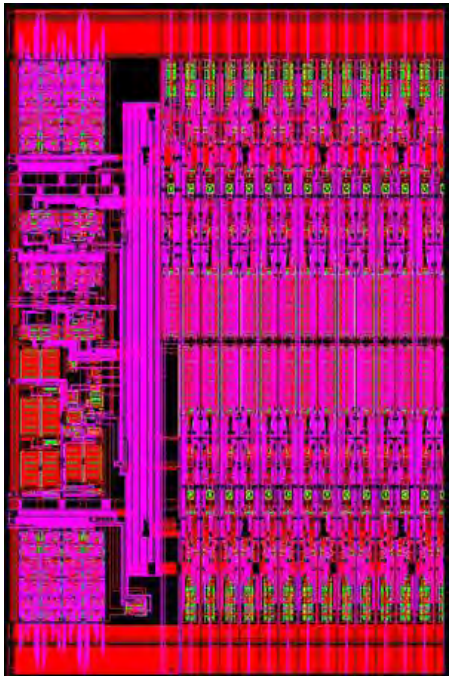


Abstract

- EMC protection elements experienced significant heating after surge impulses (253 W).
- The thermal behavior of the protection elements was modeled with the method of finite elements (FEM). COMSOL Multiphysics® *Heat Transfer Module*

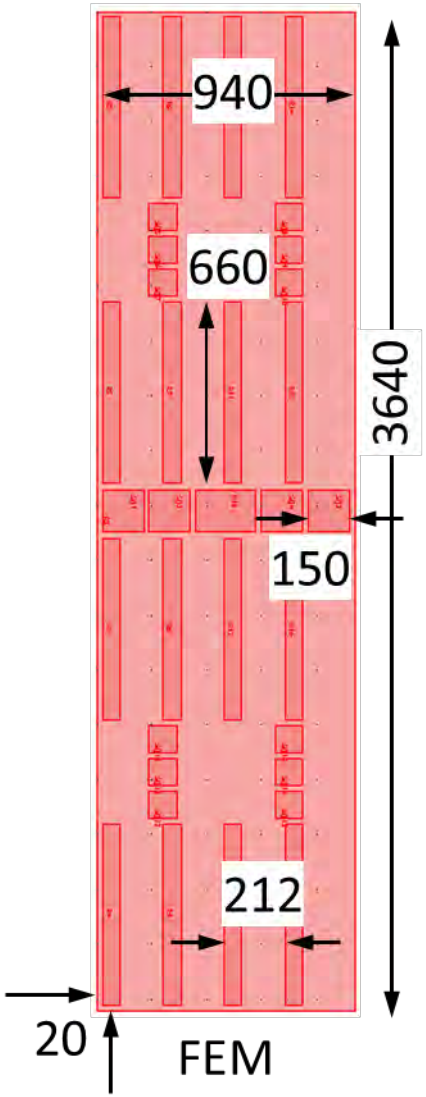
  Equation solved: $\rho c_P \frac{\partial T}{\partial t} - \nabla\left(k \nabla T\right) = Q$
- The FEM results led to a compact model to allow for design and simulation with simpler tools.
- The company HMT used our results for a new series of protection elements. Sensor circuit and protection elements are now integrated in a single ASIC design.

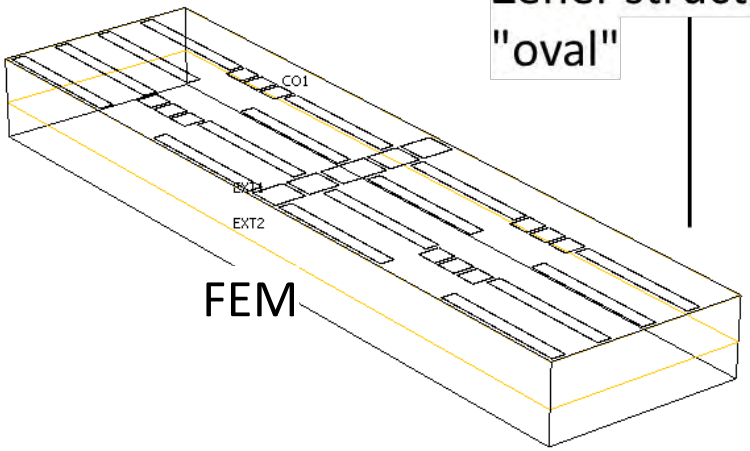
HMT
microelectronic AG

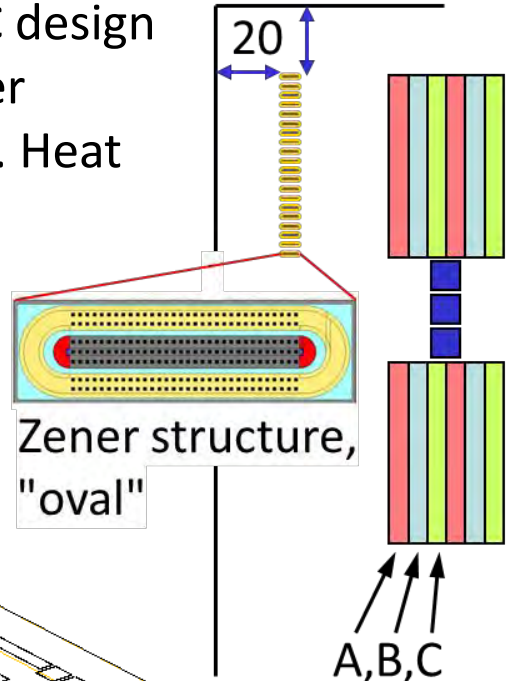


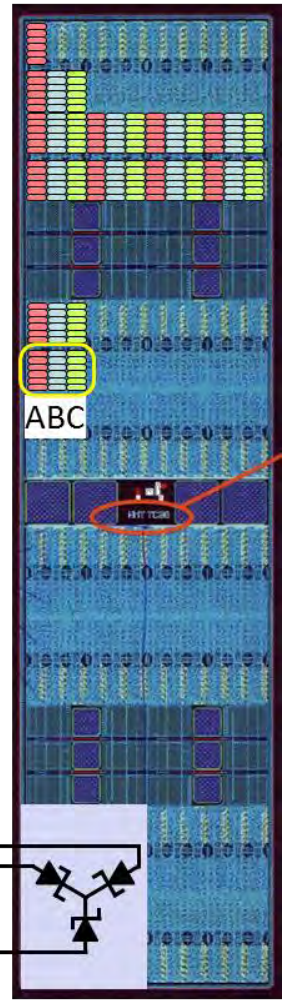
Test Chip 30

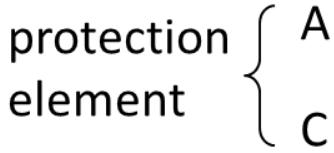
FEM model and ASIC design of a test chip of Zener protection elements. Heat is dissipated in the "Zener-A-bands".



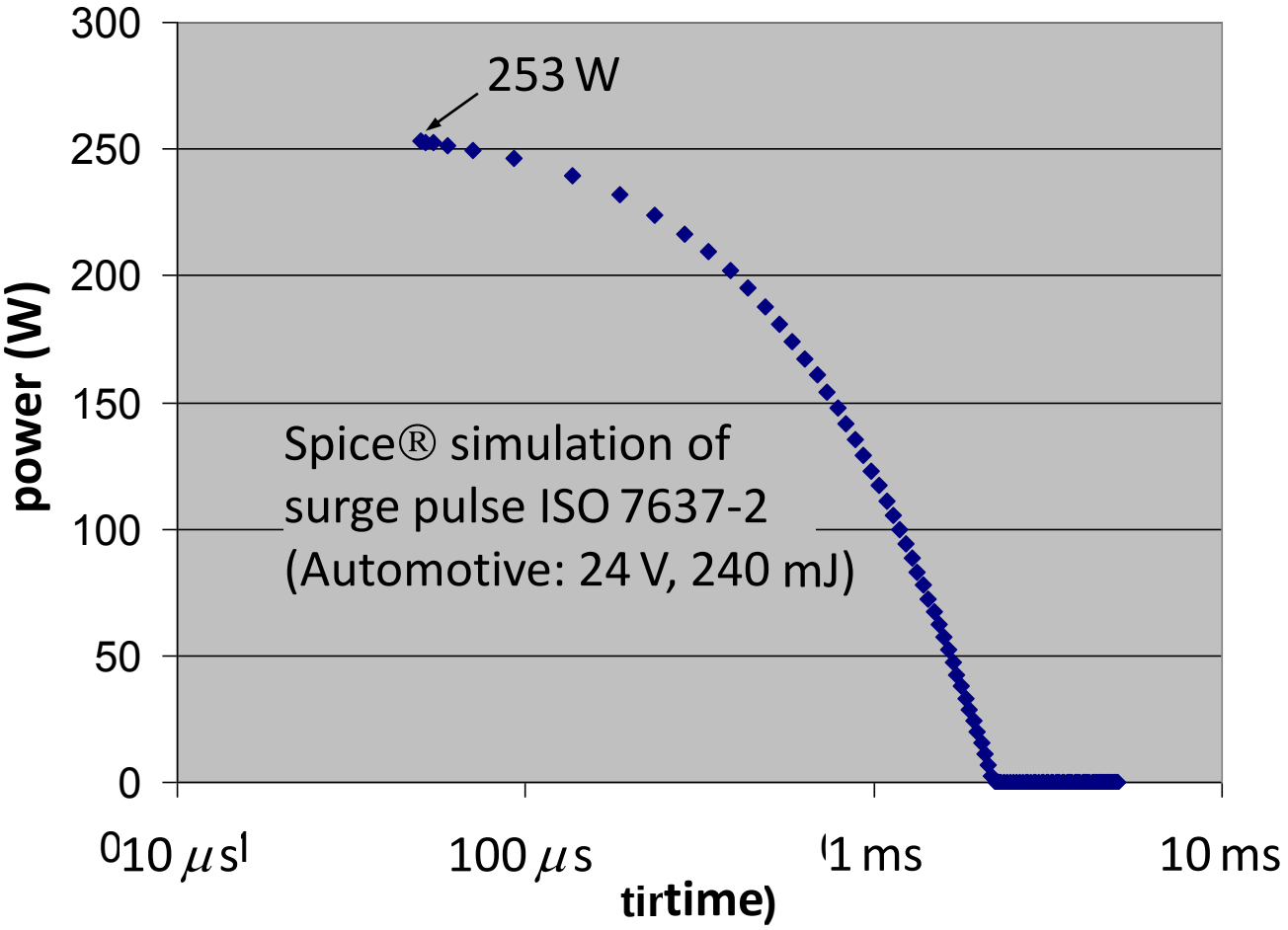








Surge Pulse

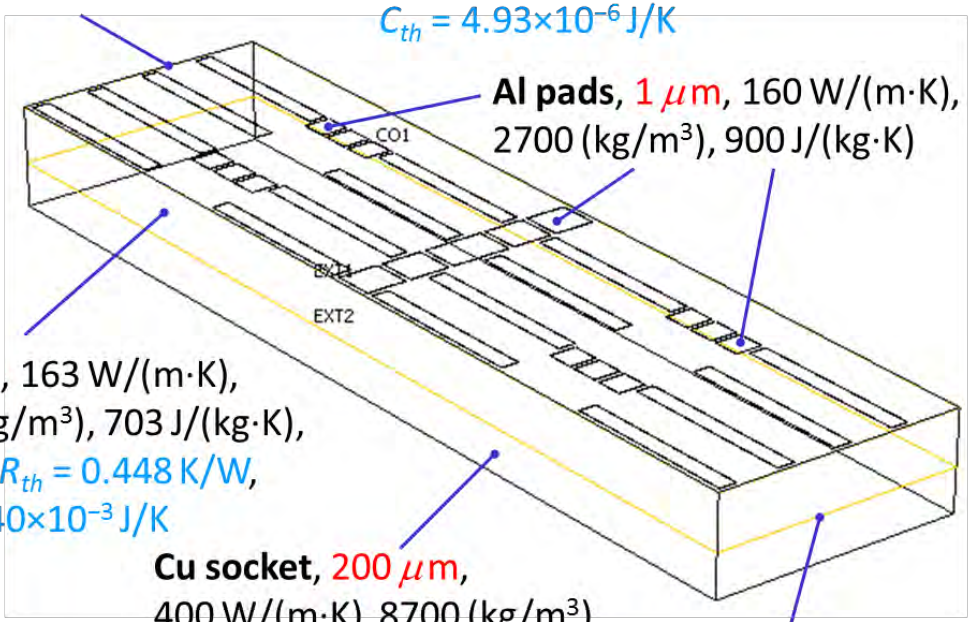


ISO 7637-2 dissipates most heat of all studied standards

Model Data

buried SiO_2, 0.5 μm,
1.38 W/(m·K), 2203 (kg/m^3),
703 J/(kg·K), R_{th} = 0.106 K/W,
C_{th} = 2.65×10^{-6} J/K

Au wires attached to Al pads,
$\varnothing$ = 50 μm, L = 1000 μm,
300 W/(m·K), 19300 (kg/m^3),
130 J/(kg·K), R_{th} = 1700 K/W,
C_{th} = 4.93×10^{-6} J/K



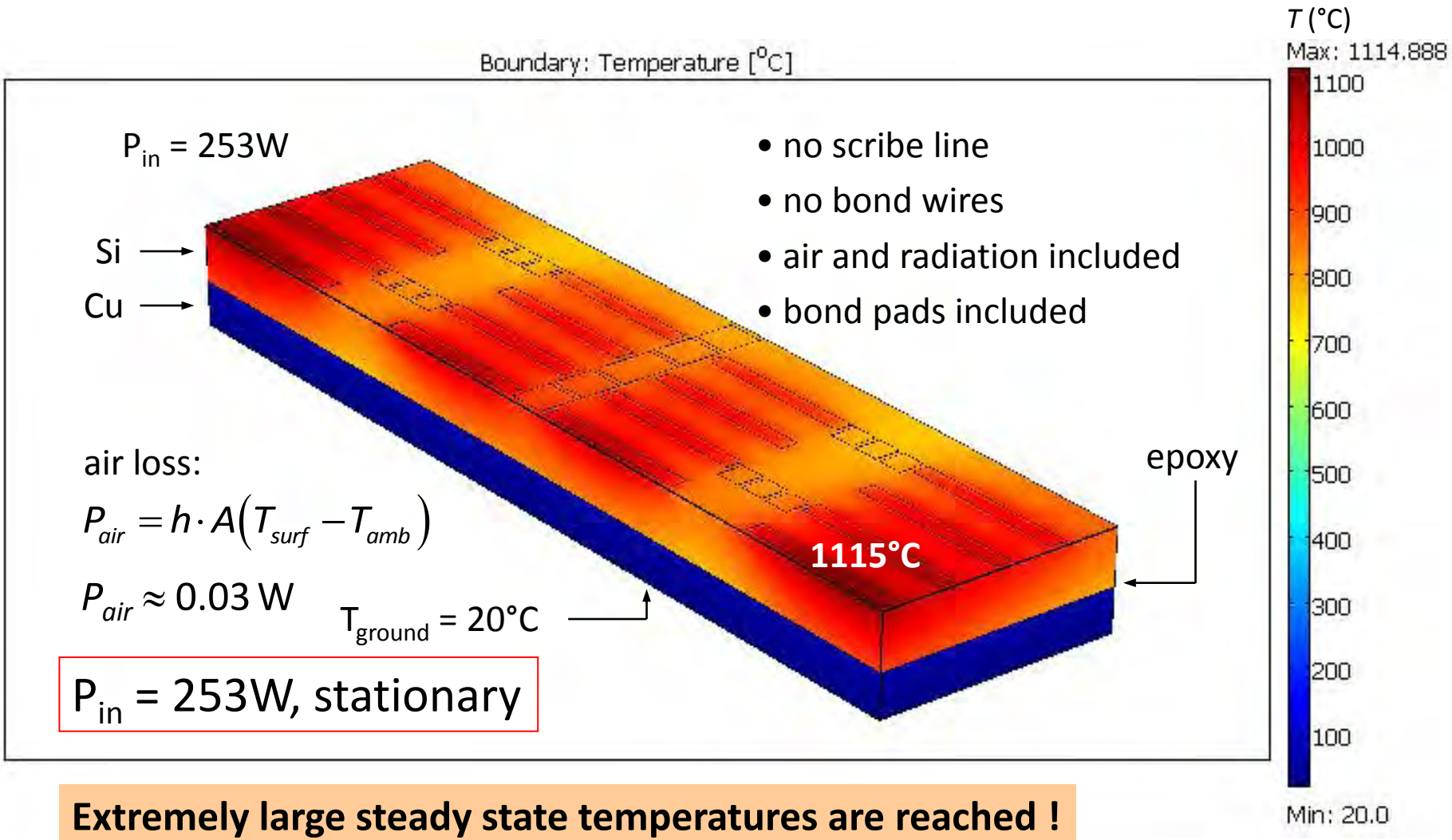
Al pads, 1 μm, 160 W/(m·K),
2700 (kg/m^3), 900 J/(kg·K)

Si die,
250 μm, 163 W/(m·K),
2330 (kg/m^3), 703 J/(kg·K),
ε = 0.2, R_{th} = 0.448 K/W,
C_{th} = 1.40×10^{-3} J/K

Cu socket, 200 μm,
400 W/(m·K), 8700 (kg/m^3),
385 J/(kg·K), R_{th} = 0.146 K/W,
C_{th} = 2.29×10^{-3} J/K

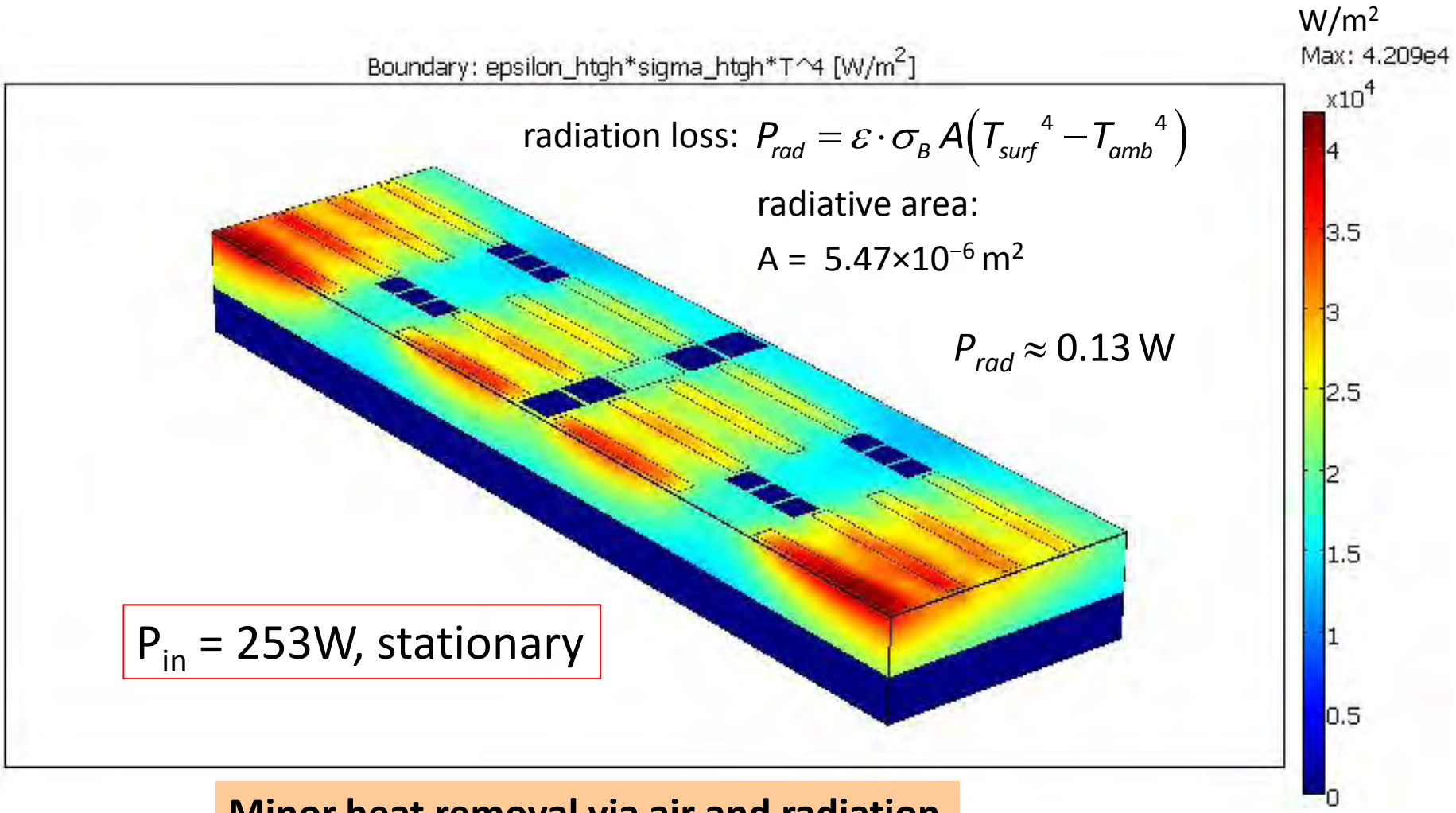
epoxy adhesive, 10 μm,
1.0 W/(m·K) ! 1400 J/(kg·K),
R_{th} = 2.92 K/W, $C_{th} \approx 7\times10^{-5}$ J/K

Surface Temperature



Extremely large steady state temperatures are reached !

Radiation



radiation loss: $P_{rad} = \varepsilon \cdot \sigma_B A\left(T_{surf}{}^4 - T_{amb}{}^4\right)$

radiative area:

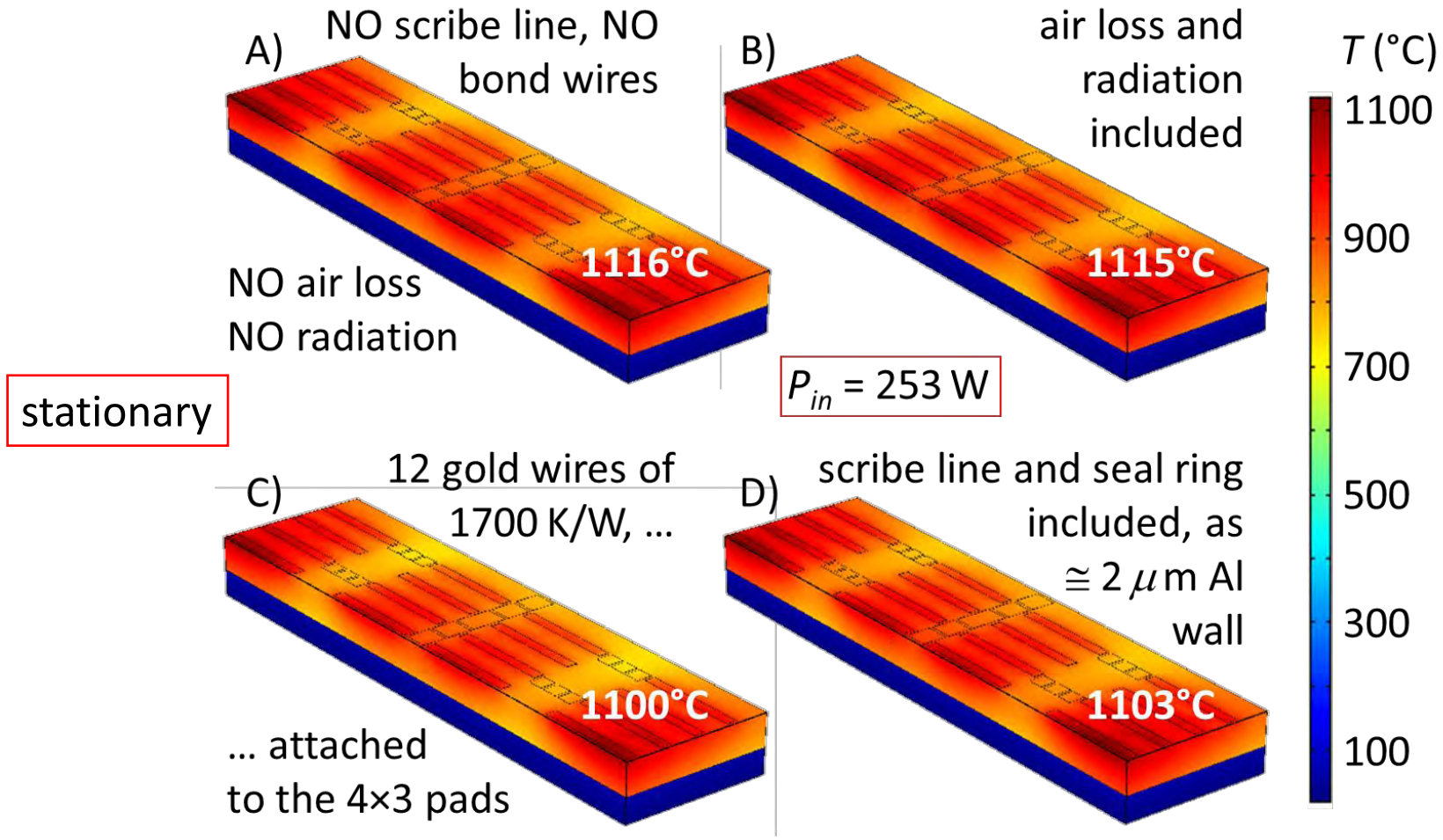
A = 5.47×10^{-6} m^2

$P_{rad} \approx 0.13$ W

P_{in} = 253W, stationary

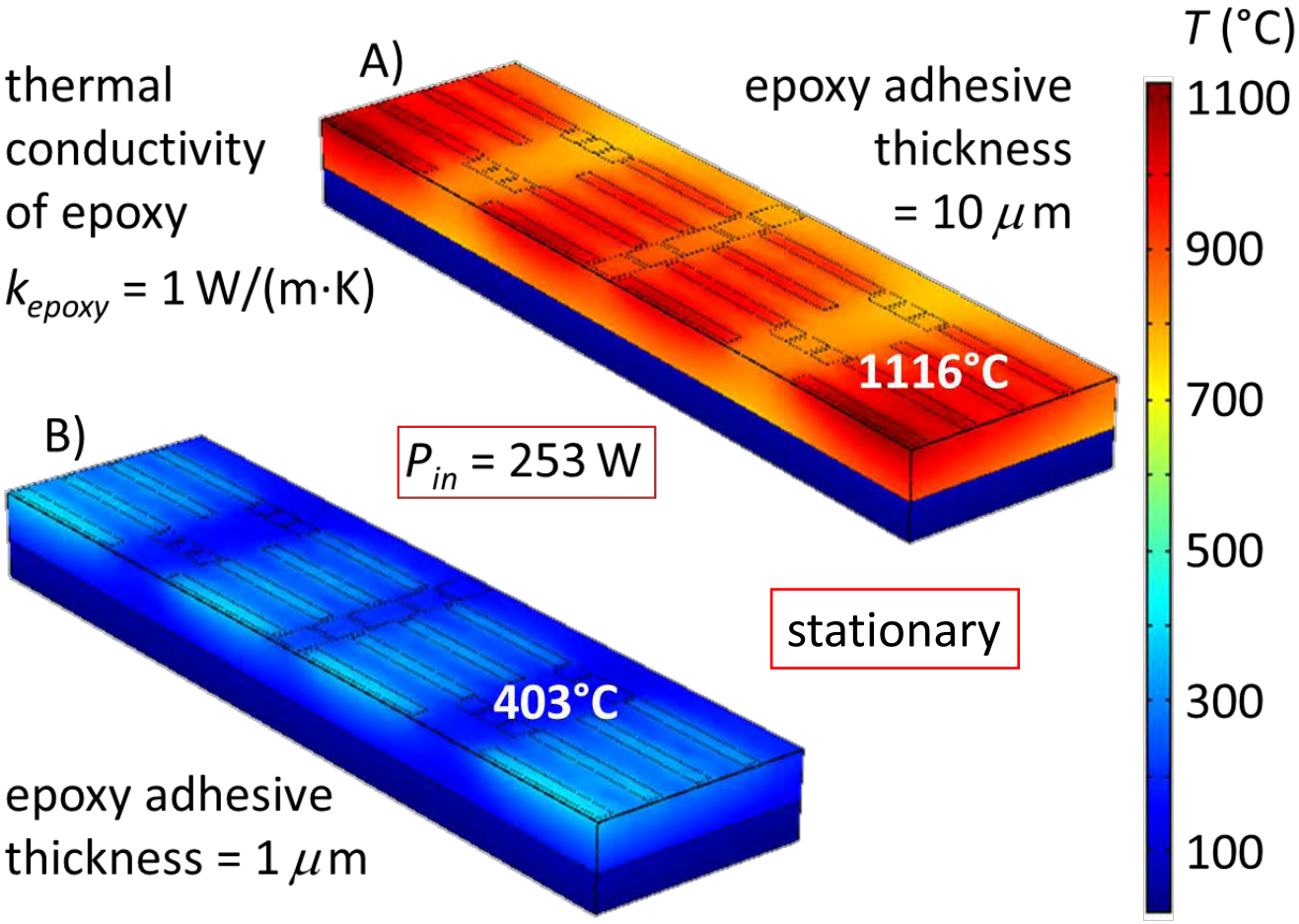
Minor heat removal via air and radiation

Heat Channels



T_{max} is governed by contact to base

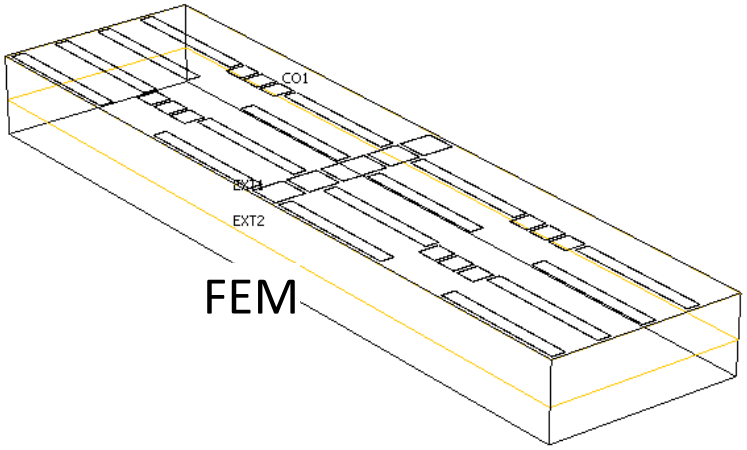
Epoxy Resistance



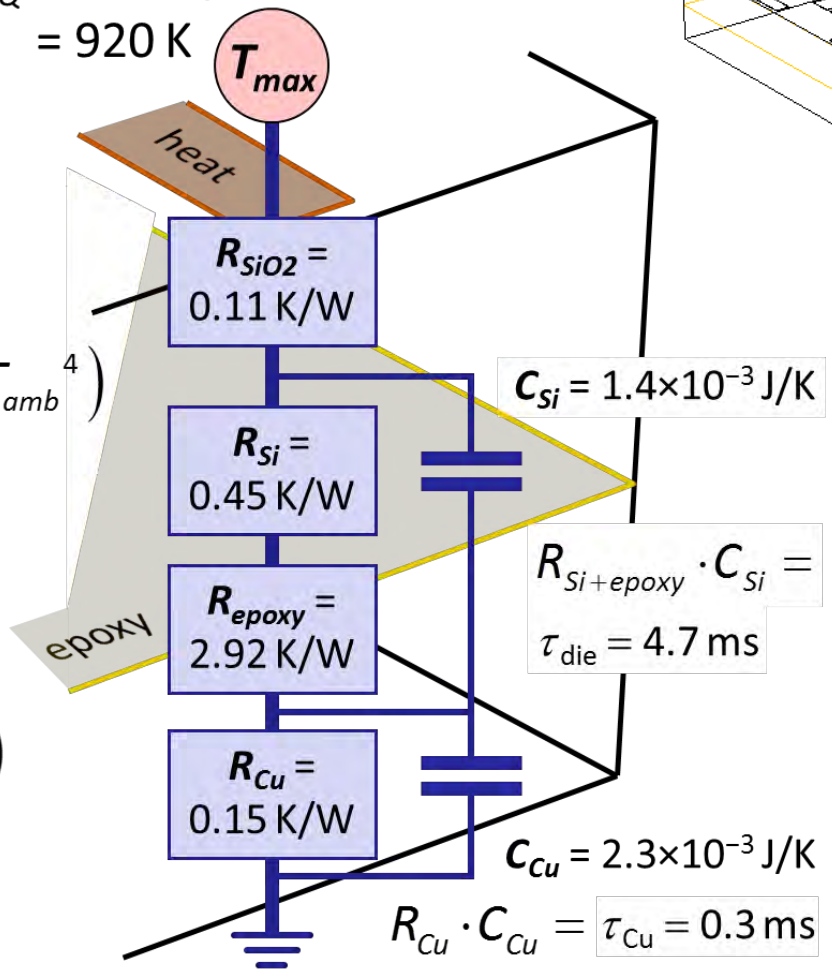
Decrease of contact resistance by a factor 10 reduces T_{max} considerably !

Ab Initio 1D-Model

$\Delta T = R_{th} \cdot J_Q$ = 3.63 K/W × 253 W
= 920 K



FEM



radiative loss of chip surface

$\varepsilon \cdot \sigma_B A\left(T_{surf}^{\ 4} - T_{amb}^{\ 4}\right)$

$= P_{rad} \approx 0.13\,\text{W}$

conductive loss to air

$h \cdot A\left(T_{surf} - T_{amb}\right)$

$= P_{air} \approx 0.03\,\text{W}$

$C_{Si} = 1.4\times10^{-3}$ J/K

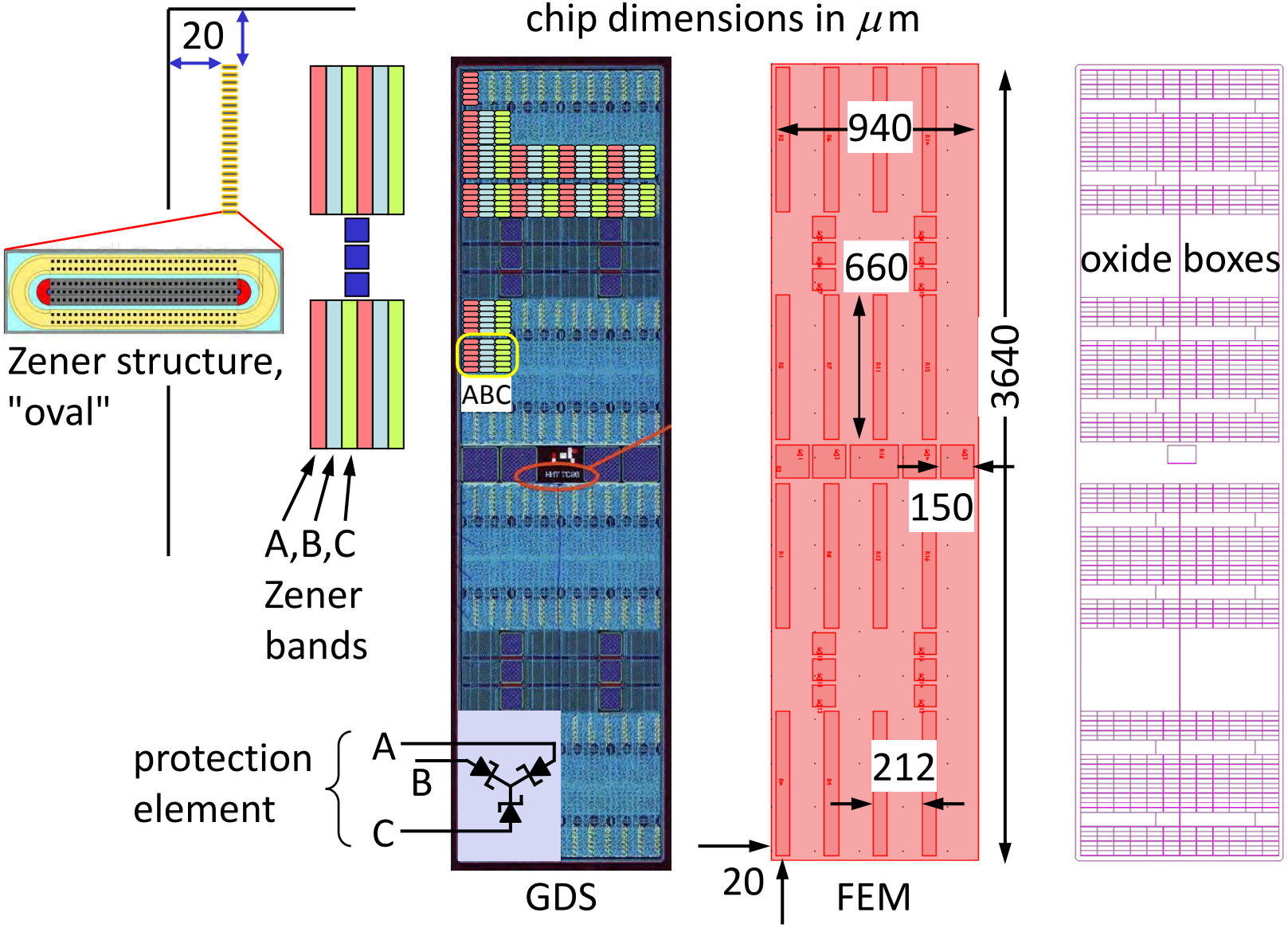
$R_{Si+epoxy} \cdot C_{Si} = \tau_{die} = 4.7$ ms

$C_{Cu} = 2.3\times10^{-3}$ J/K

$R_{Cu} \cdot C_{Cu} = \tau_{Cu} = 0.3$ ms

Test Chip 30

chip dimensions in μm



p-n Heat

2.10.7 ESD13

6.2V Zener Diode – for ESD only
P^+ on N-Extension

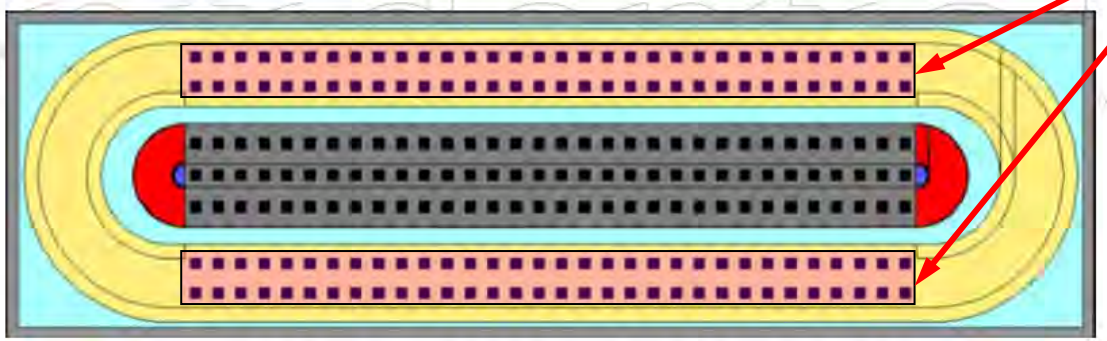
Scalable device similar to DZPENX1, 8<IM<25 designed for ESD purposes

Parameter	Param. name	Condition	Min	Typical @ 25°C	Max	Unit
Reverse Breakdown Voltage Ratings	V_{KA}	I_K=0.5µA	6.13	6.28	6.42	V
Trench isolation	$\|V_{max}\|$				100	V
Handle potential influence on V_{KA}	$\|dV_{KA}\|$	-100V<V_{AH}<100V 0.5µA<I_K<1mA			0.05	V
Leakage current per module	I_{KA}	V_{KA}=5.5V IM=1 *1 *2		0.5		nA
TLP reverse current IM=1	I_{TLPrev}			0.19		A
TLP reverse voltage	V_{TLPrev}	I_{TLPrev} *2		15		V
TLP forward voltage	V_{TLPfwd}		10			V
MM per module	V_{MMrev}	JEDECA 115A *3		30		V
HBM per module	V_{HBM}	100pF 1.5kOhm AIC Q100 accept		350		V

*1 T_{pulse}=80ns T_{rise} =10ns *2 <10% I_{KA} Increase V_{KA}=5V *3 DIP48 600mil ceramic package

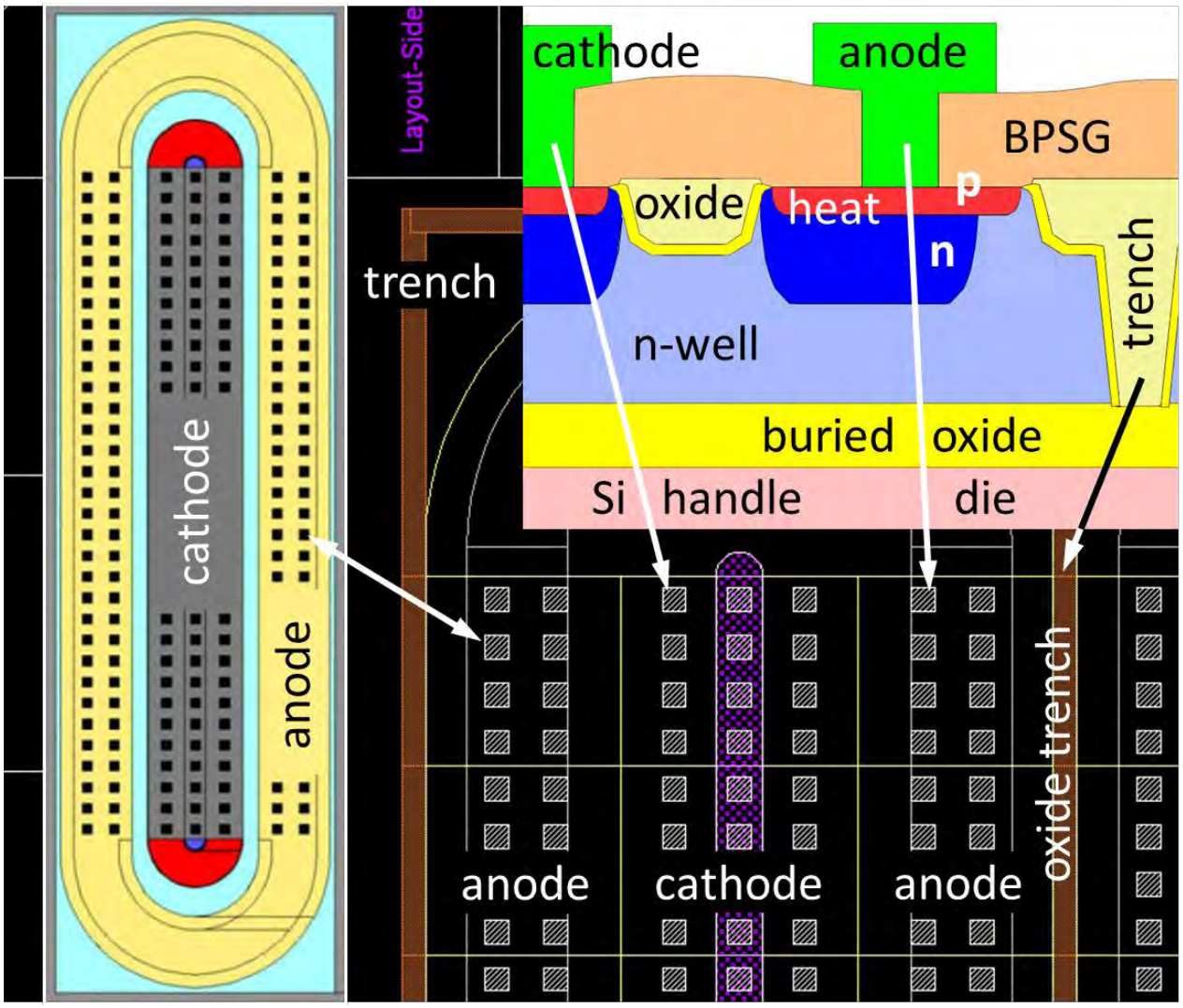
Layout Cell:
Dimensions for min device (8 modules)
84.7um x 22.8um
Scale 1500:1

Module size:
6.4um x 22.8 um



Details of TC30

Zener structure, "oval"



Layer Data

Table 3: Conductive Layers

Conductive Layers	Resistivity				Thickness			
	Min	Typ	Max	Unit	Min	Typ	Max	Unit
N+Poly Gate	21	26	31	Ω/sq		350		nm
Poly 2	1600	2000	2400	Ω/sq		200		nm
Metal1 TiTiN/AlSiCu/TiN	54.5	61.5	68.6	mΩ/sq	650	700	750	nm
Metal2 Ti/AlSiCu/TiN	31	38	45	mΩ/sq	950	1000	1050	nm
Metal3 Ti/AlSiCu/TiN	12.6	14.6	16.6	mΩ/sq	1950	2000	2050	nm

>95%

sheet resistance of Al: $\rho/d = 2.8\times10^{-8}/1\times10^{-6} = 30$ mΩ/□

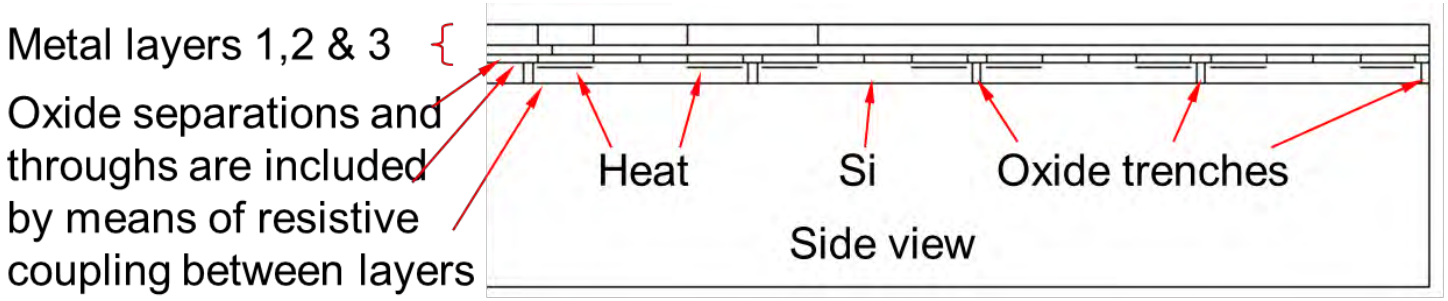
Fundamental Technological Parameters

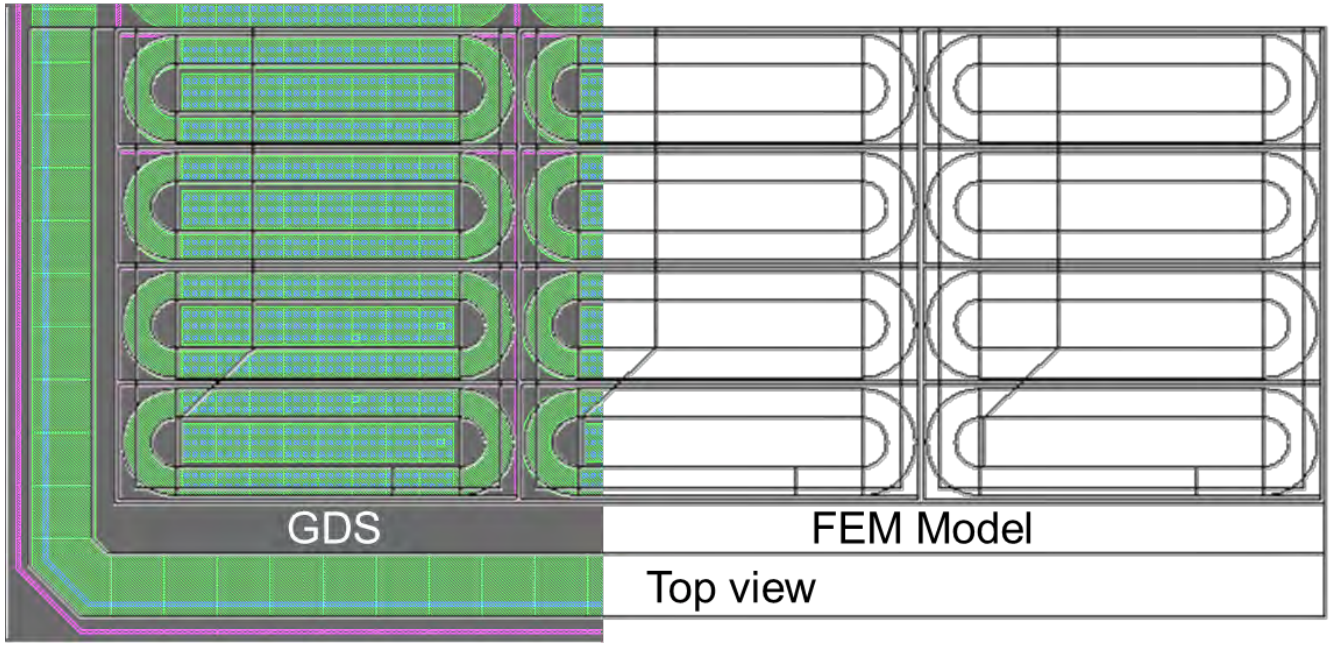
The fundamental technological parameters describe the parameters which are essential for the technology. The compliance of these parameters is the base for achieving the guaranteed quality of an integrated circuit. Furthermore, they are the prerequisite for achieving a reliability on high level. Fundamental technological parameters are subject to statistical process control on test or product wafers.

In this section the fundamental parameters are listed which are checked during the wafer process. Furthermore, fundamental parameters for the description of the essential electrical characteristics of the devices can be found in the chapter PCM (Process Control Monitor).

thermal conductivity of titanium ≈ 22W/(m·K); layer sheet resistance Ω/□ is that of not pure Al

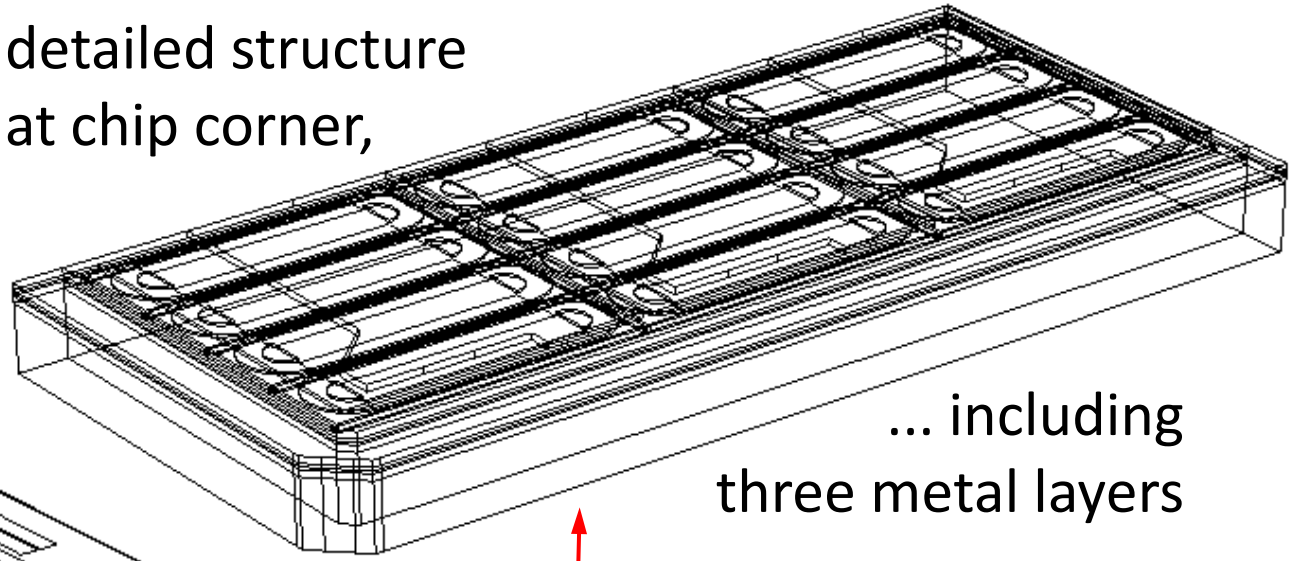
Layer Structure



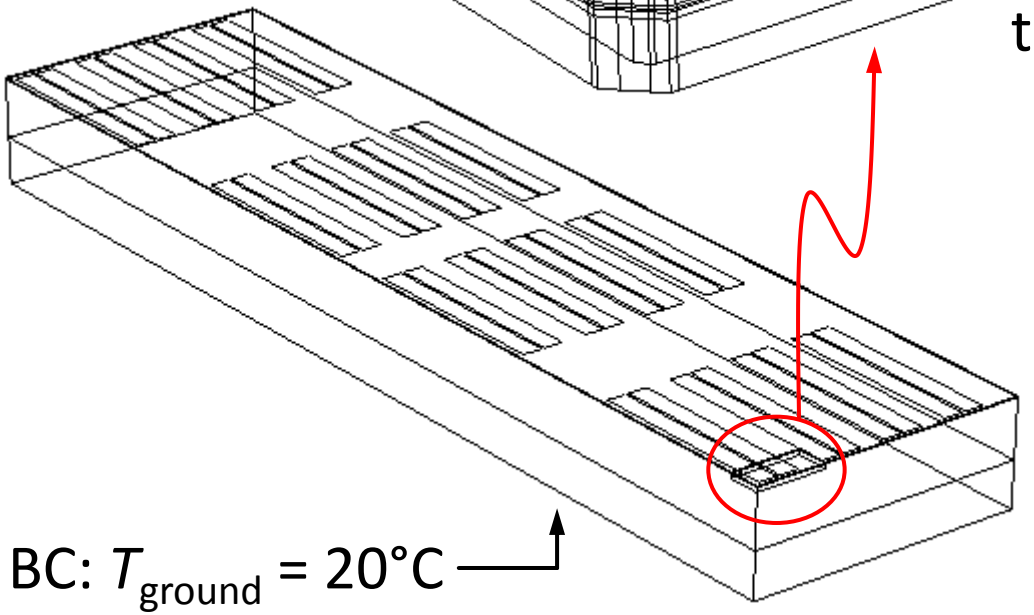


Detailed Model

detailed structure
at chip corner,



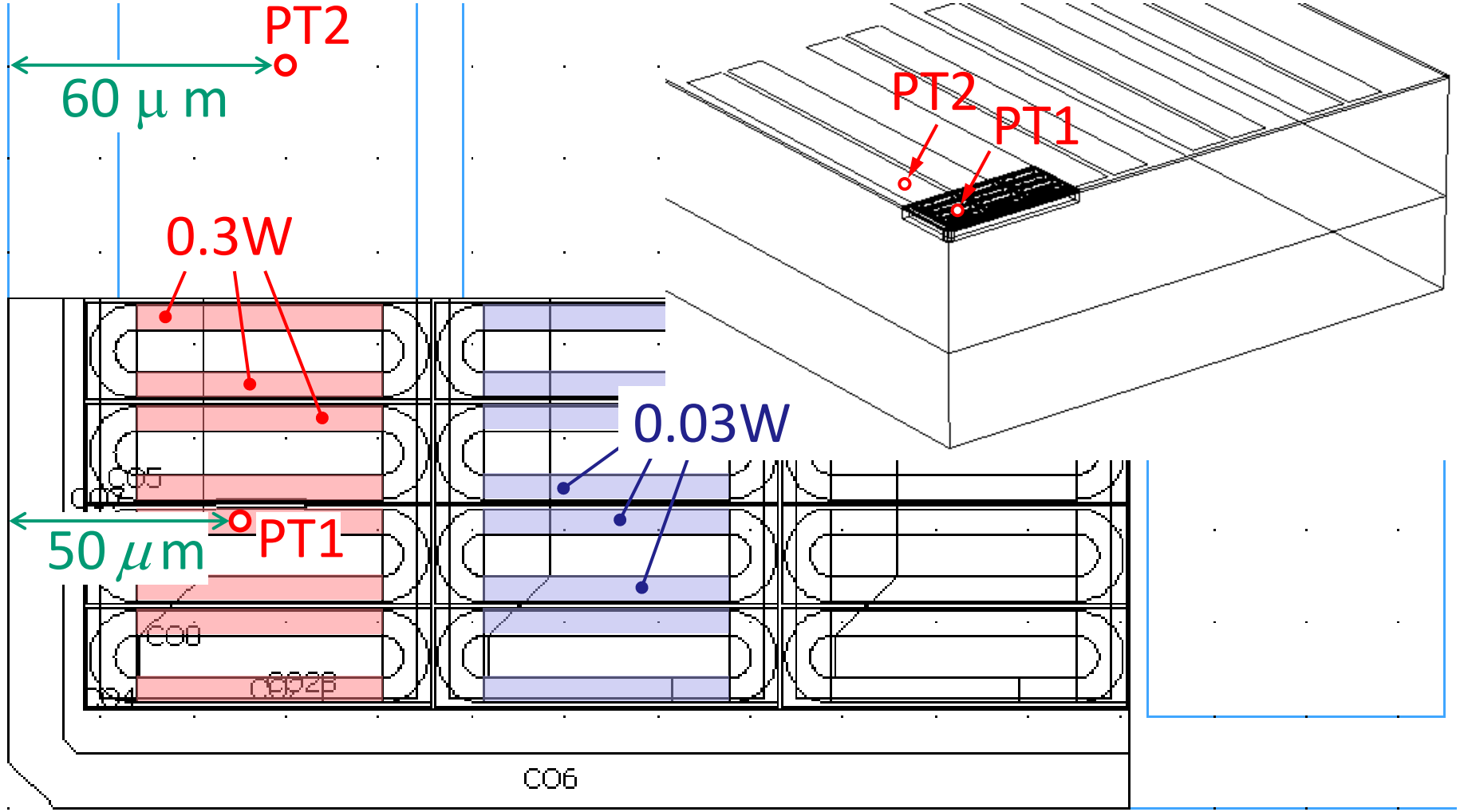
... including
three metal layers



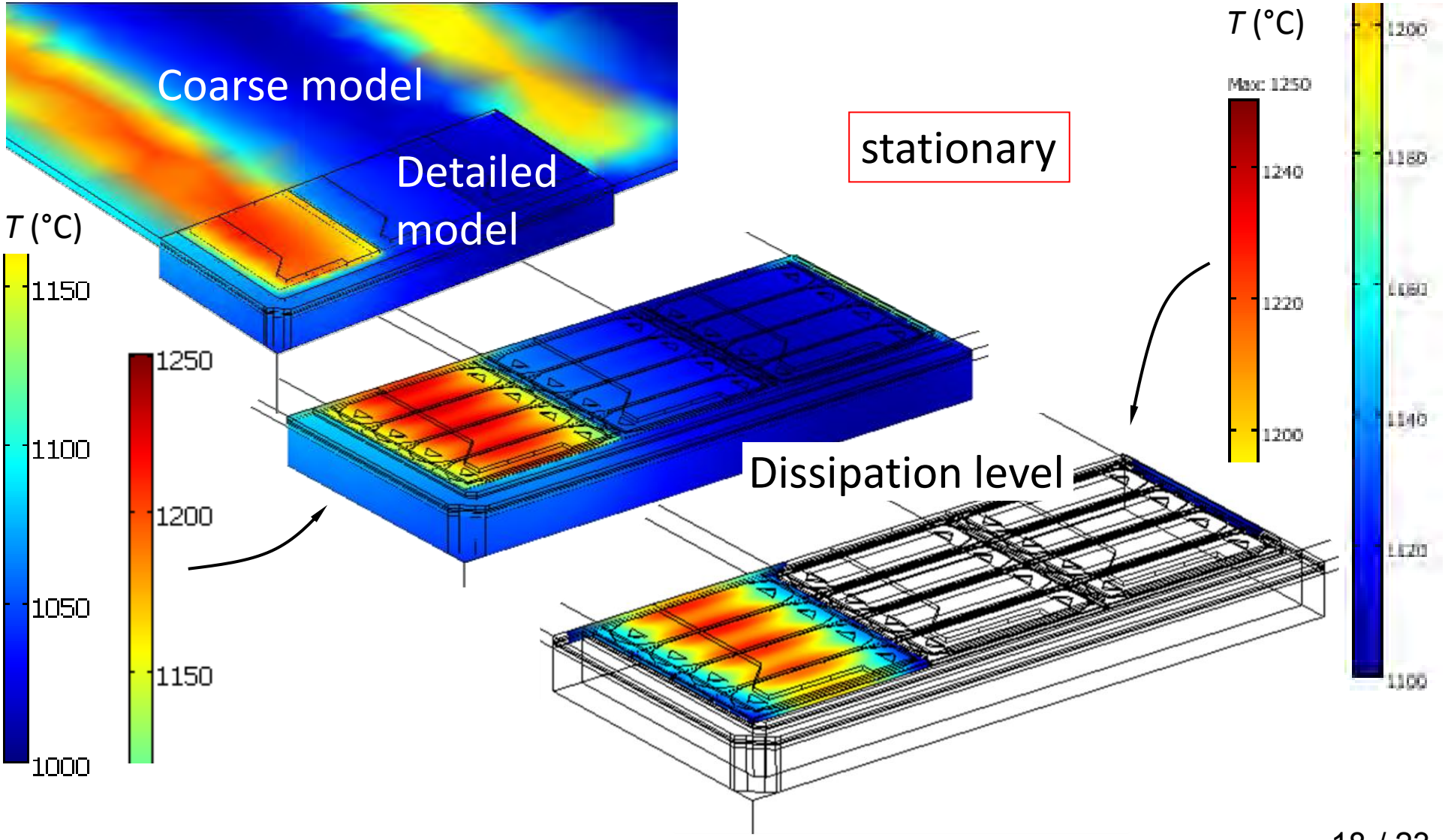
coarse test
chip model

BC: T_{ground} = 20°C

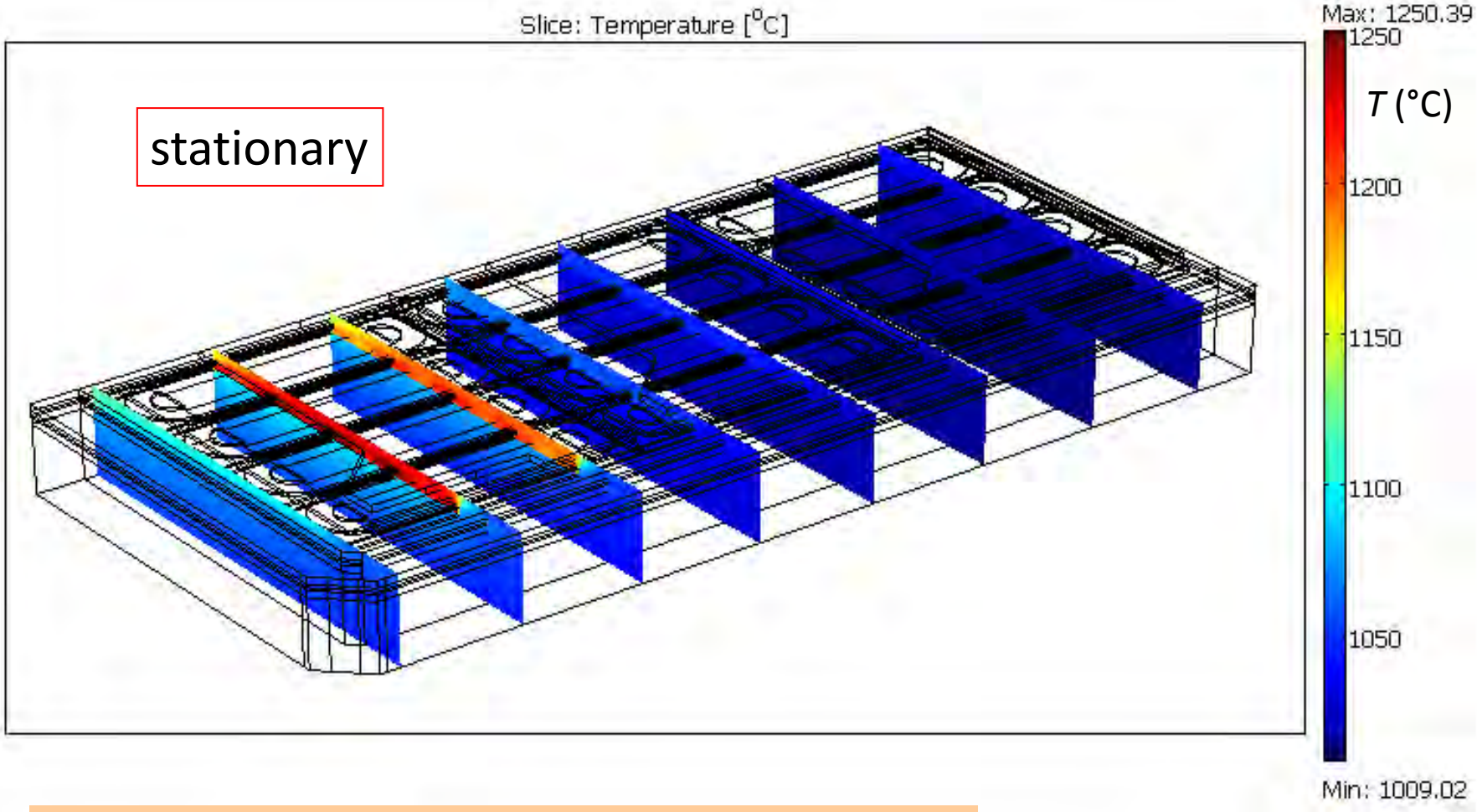
Heat Input



Active Layer Temp.



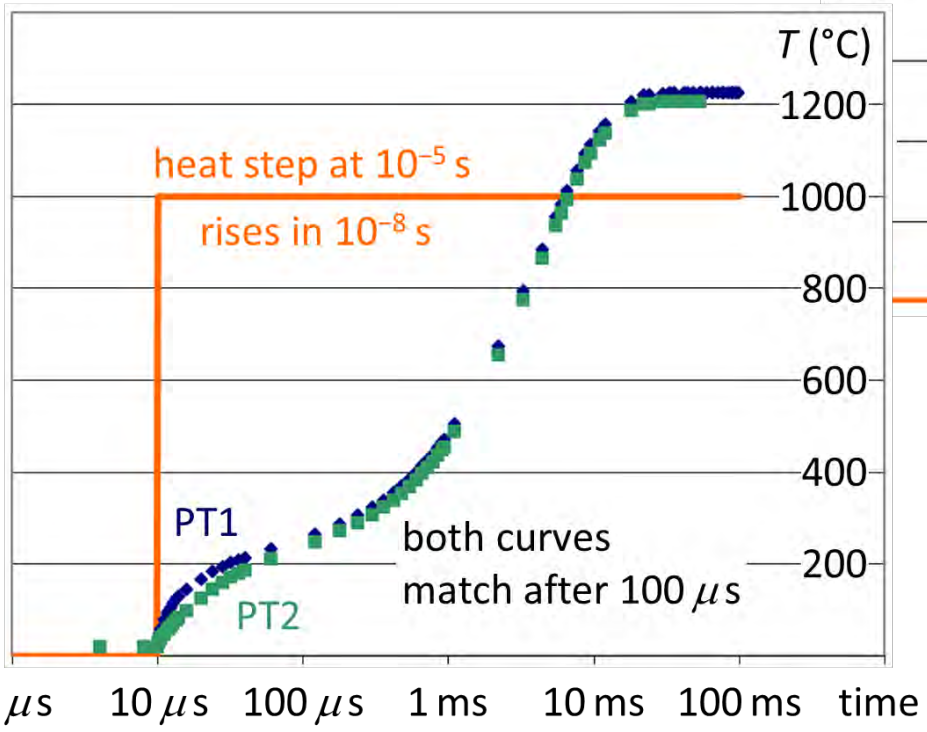
Oxide Barrier

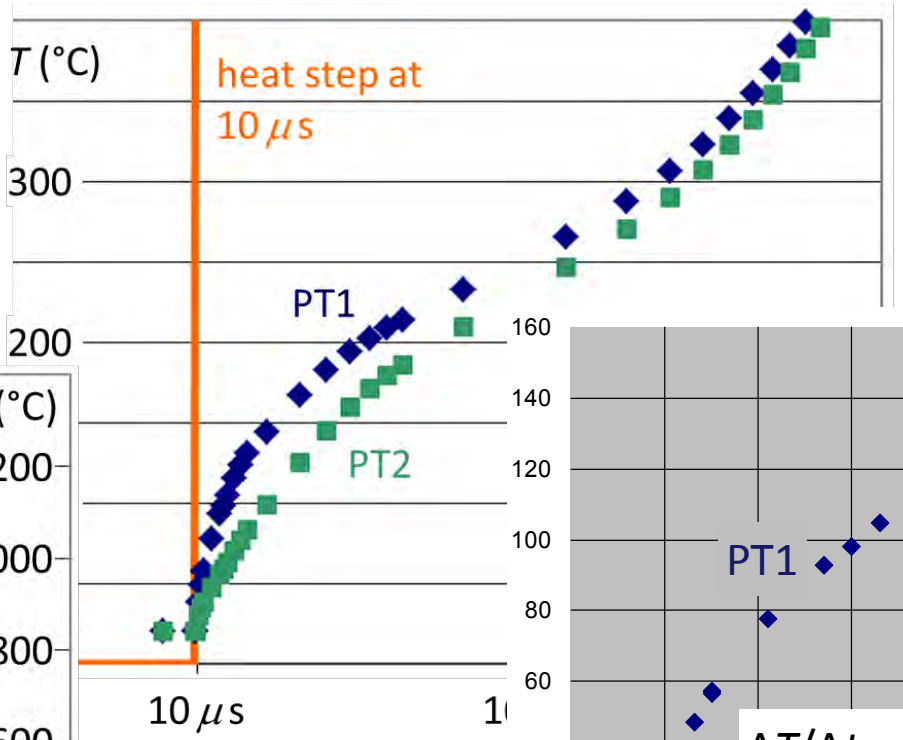


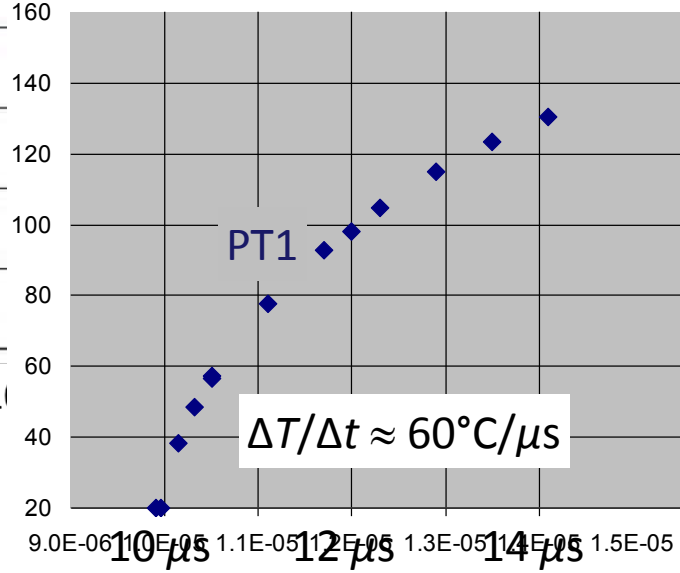
Oxide layers and trenches form thermal barriers !

Heat Step

transient







Very fast initial Temp. increase !

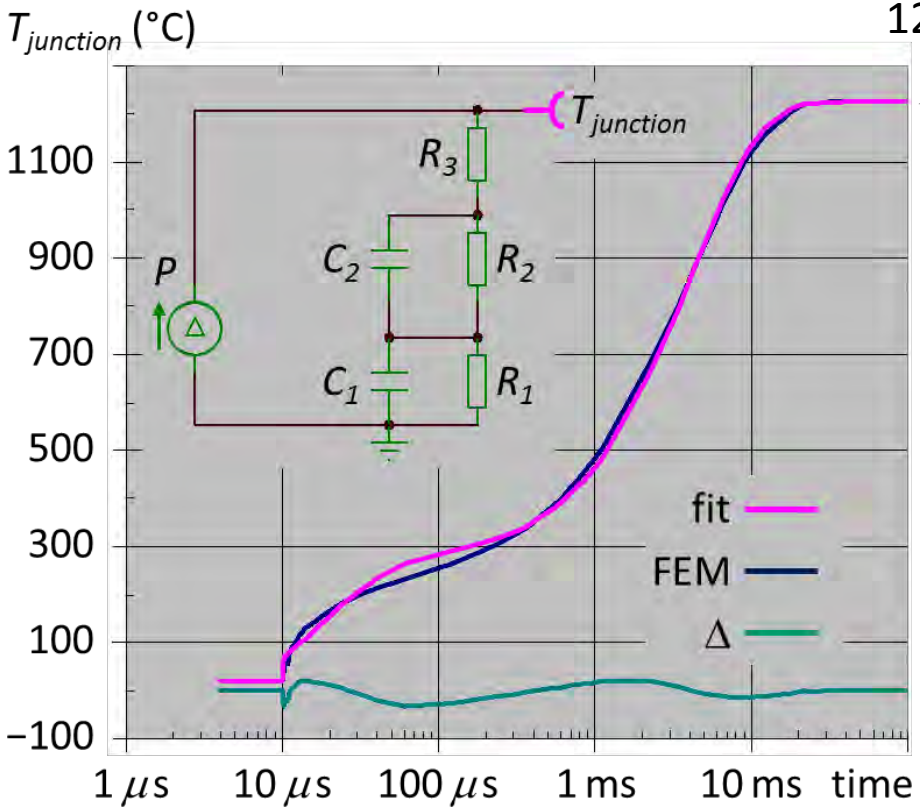
Compact Model

$$T_J(t) = T_G + T_1 \cdot \left(1 - e^{-\frac{t}{R_1 \cdot C_1}}\right) + T_2 \cdot \left(1 - e^{-\frac{t}{R_2 \cdot C_2}}\right) + T_3$$

transient

$$R_{tot} = R_1 + R_2 + R_3 = \frac{T_1 + T_2 + T_3}{P}$$

BC: T_J (t=∞) = 1225°C (FEM)



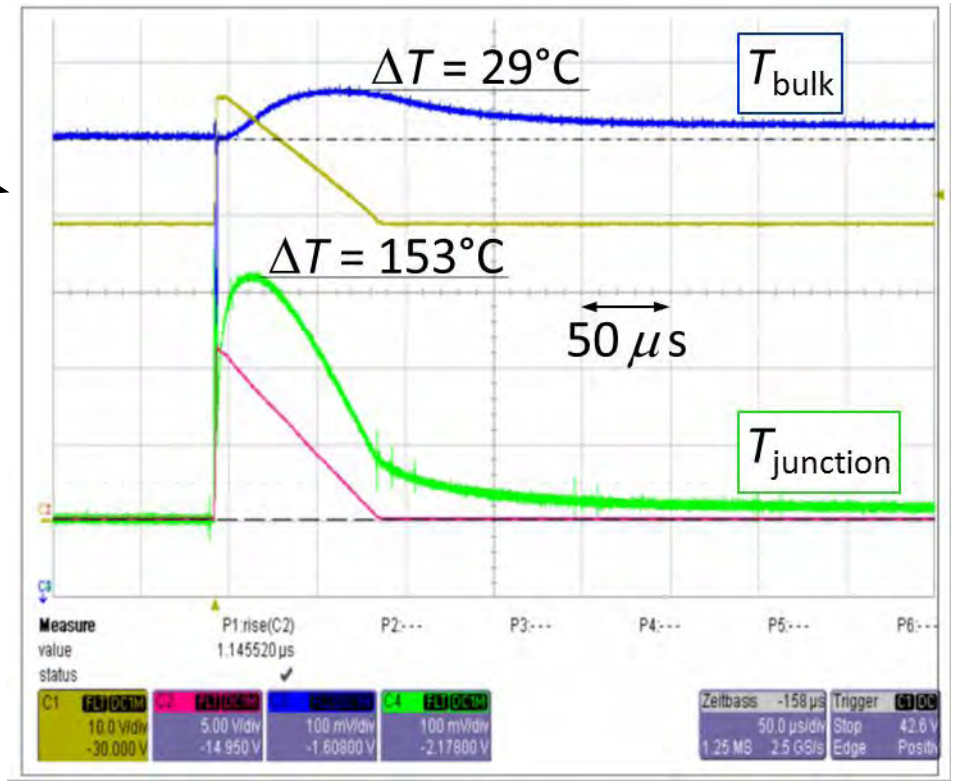
Parameter	Value	Unit
P	253	W
$T_J = T_G + T_1 + T_2 + T_3$	1225 ✔	°C
$T_3 = P \cdot R_3$	48	K
R_3 "oxide trench"	0.19	K / W
$T_2 = P \cdot R_2$	199	K
$\tau_2 = R_2 \cdot C_2$	1.8×10^{-5}	s
C_2 (fit) "active silicon"	2.3×10^{-5}	J / K
R_2 (fit) "buried oxide"	0.79	K / W
$T_1 = P \cdot R_1$	958	K
$\tau_1 = R_1 \cdot C_1$	4.2×10^{-3}	s
C_1 (fit) "die + epoxy"	1.1×10^{-3}	J / K
R_1 (fit) "die + epoxy"	3.79	K / W

Validation

Temperature evolution of the bulk silicon and the junction during a 2.0 A surge impulse-equivalent (triangular shape). Time axis is 50 μs / div .

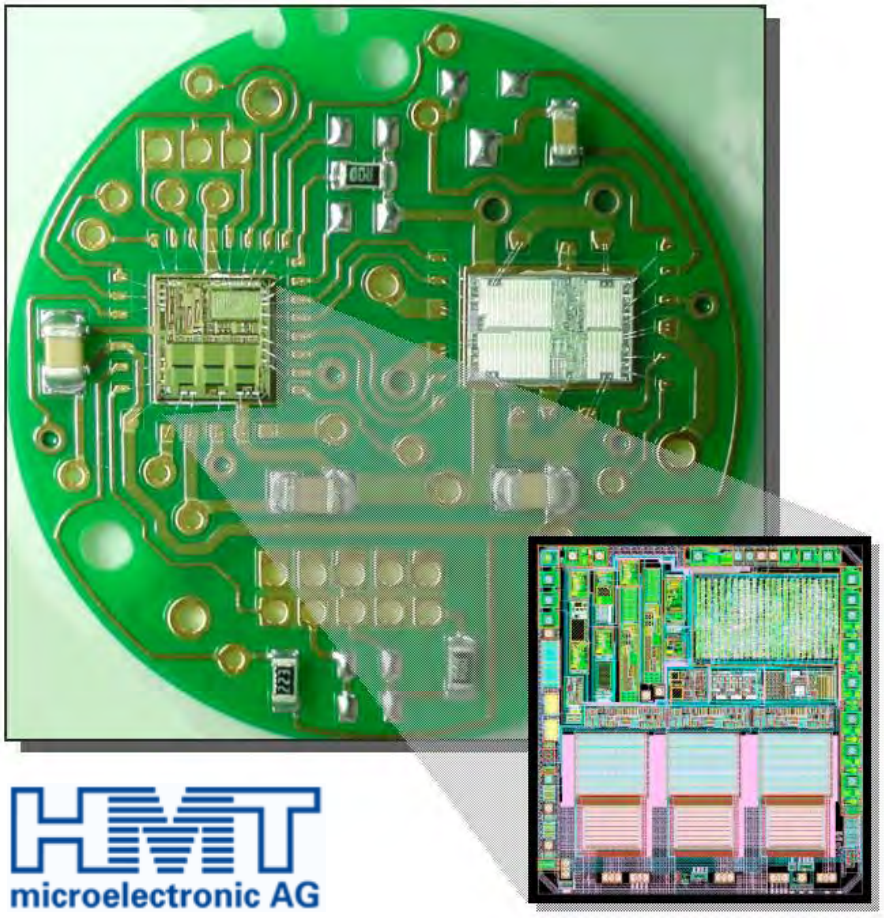
transient

Note the high junction temperature of 153°C after mere 20 μs and the ultra fast measurement !



The mechanism of heat flux and temperature evolution of the test chip is essentially understood. Material and geometry data of similar chips allow for prediction of the temperature evolution prior to FEM simulations.

Conclusions



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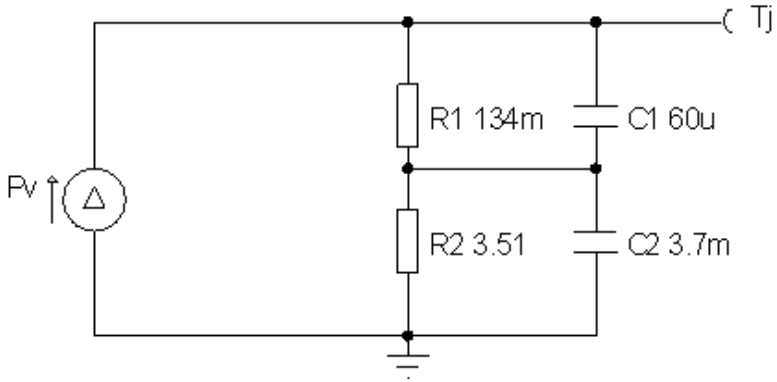
- The maximum temperature is governed by the die attach. Heat flux through bond-wires or by conduction or radiation to air is negligible.
- Oxide trenches in the active silicon layer and the buried oxide cause efficient thermal insulation.
- We were able to measure the initial temperature rise after a heat step emulating surge pulse ISO 7637-2: The junction temperature increases by $60\,\mathrm{K}/\mu\mathrm{s}$.
- A compact model based on exponential fitting reproduces the temperature evolution of the FEM simulation accurately.

Ab Initio Model

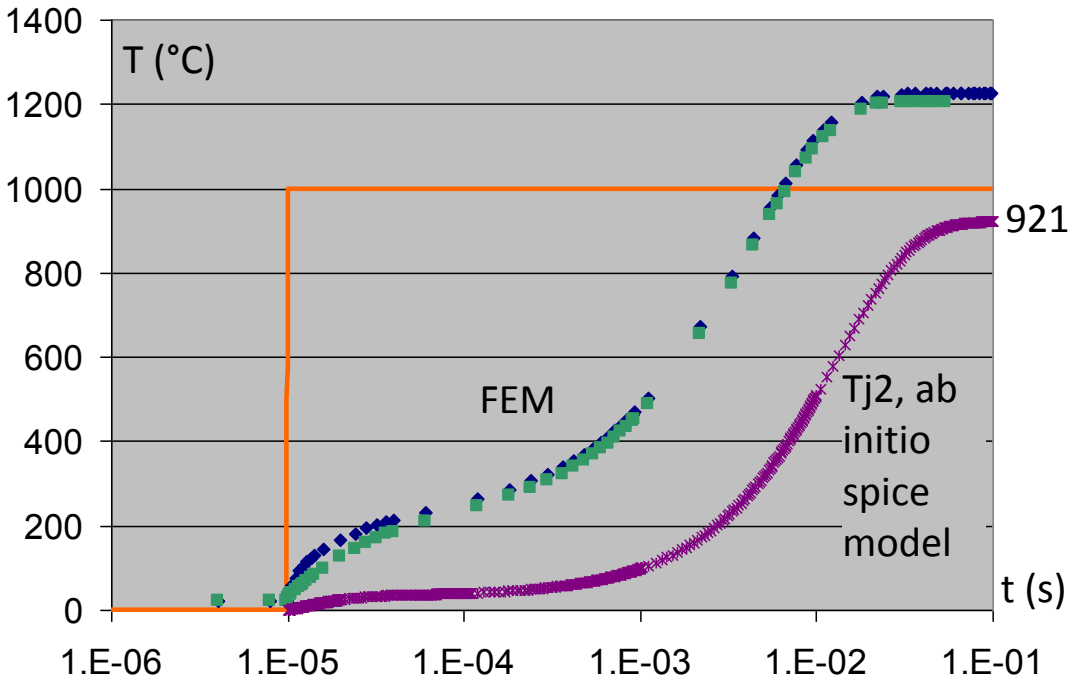
To emulate the FEM results a Spice model was created. The model consists of the active chip layer (top) and the wafer handle (bottom).



1	R_1	= 0.14	K/W
	C_1	= 6.1E-05	J/K
	τ_1	= 8.2E-06	s
	T_{j1}		
2	R_2	= 3.51	K/W
	C_2	= 3.6E-03	J/K
	τ_2	= 0.013	s
	T_{j2}	= 922	K
	P_v	= 253	W

Two-layer model: Ab initio R and C

P_{in} = 253W	top layer	b.o.	wafer	epoxy	socket
R_{th} (K/W)	0.03	0.11	0.45	2.94	0.15
C_{th} (J/K)	6.1×10^{-5}	0	1.3×10^{-3}	0	2.3×10^{-3}
	1		2		



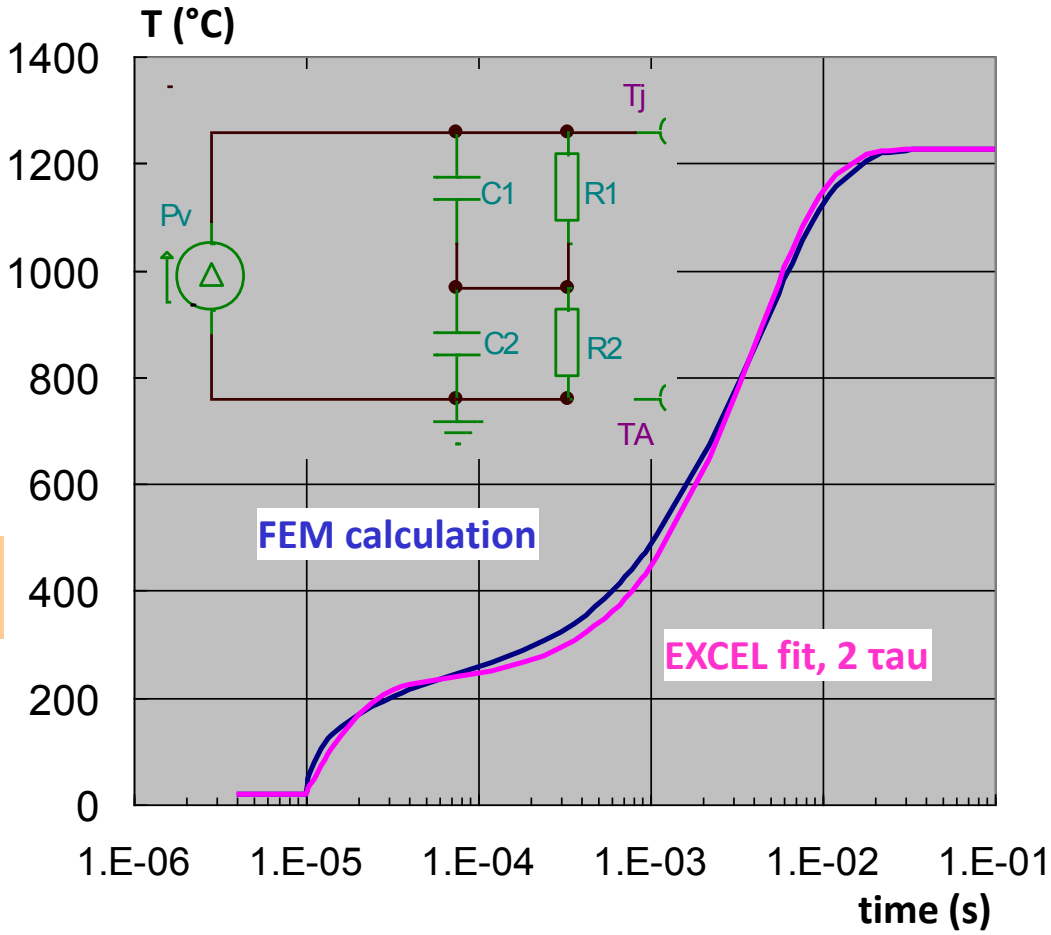
2 τau Excel Fit

The FEM thermal simulation (blue) can be fitted with two exponential functions (pink). The linear thermal equations should allow to predict the surge pulse behavior prior to FEM simulations.

parameters:

R_1	= 0.92	K/W	R_2	3.85	K/W
C_1	= 9.0E-06	J/K	C_2	1.1E-03	J/K
τ_1	= 8.2E-06	s	τ_2	4.1E-03	s
T_{j1}	= 231	K	T_{j2}	973	K
P_v	= 253	W	T_A	= 293K ≡ 20°C	

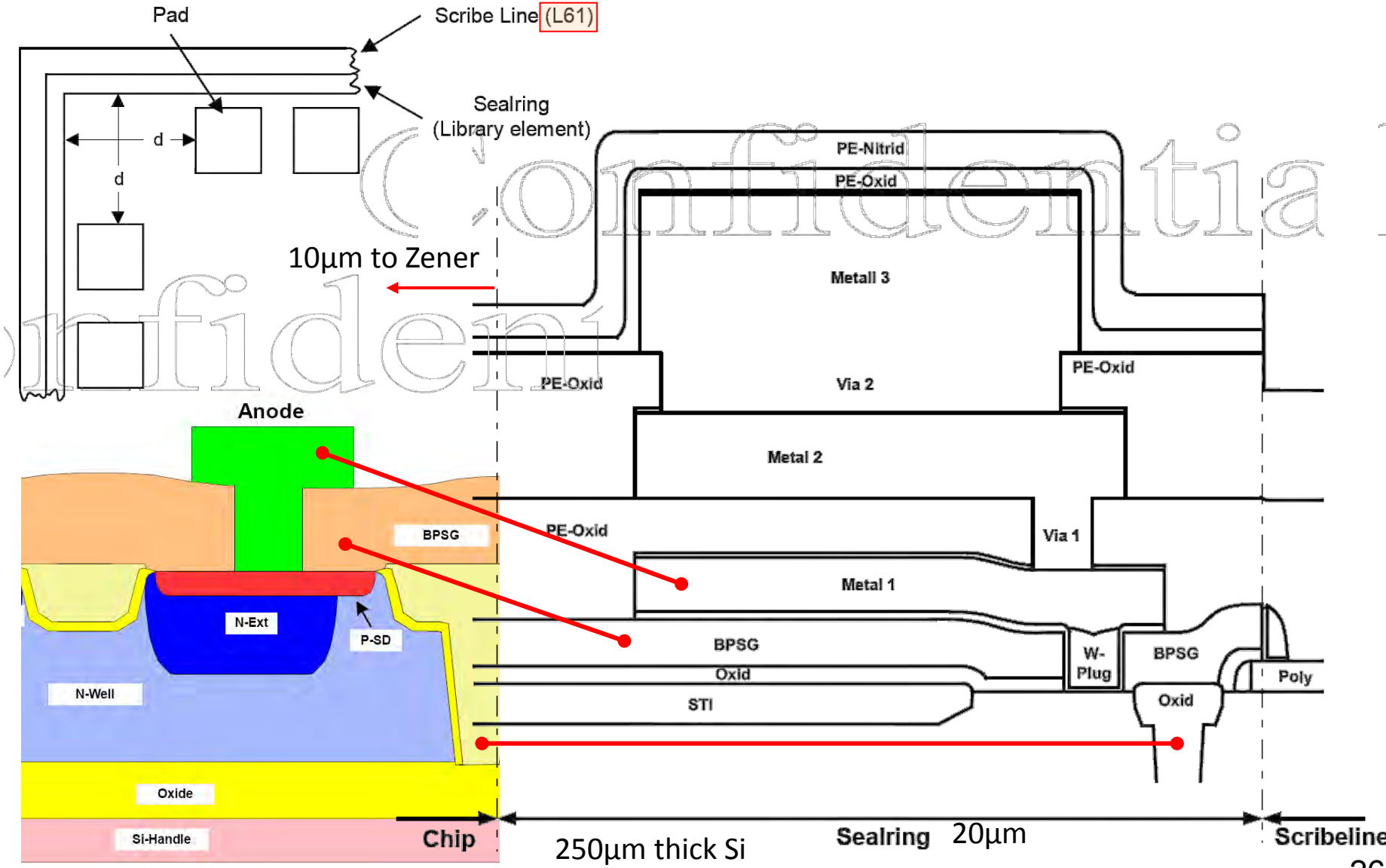
Boundary conditions (fixed parameters) were T_A = 20°C, $T_{j,\,t=\infty}$ = 1225°C (FEM) and $R_{tot} = R_1 + R_2 = (T_{j1} + T_{j2})/P_v$. The <u>three</u> fit parameters were R_1, C_1 and C_2.



$$T_{j1} = P_v \cdot R_1 \,,\; T_{j2} = P_v \cdot R_2$$

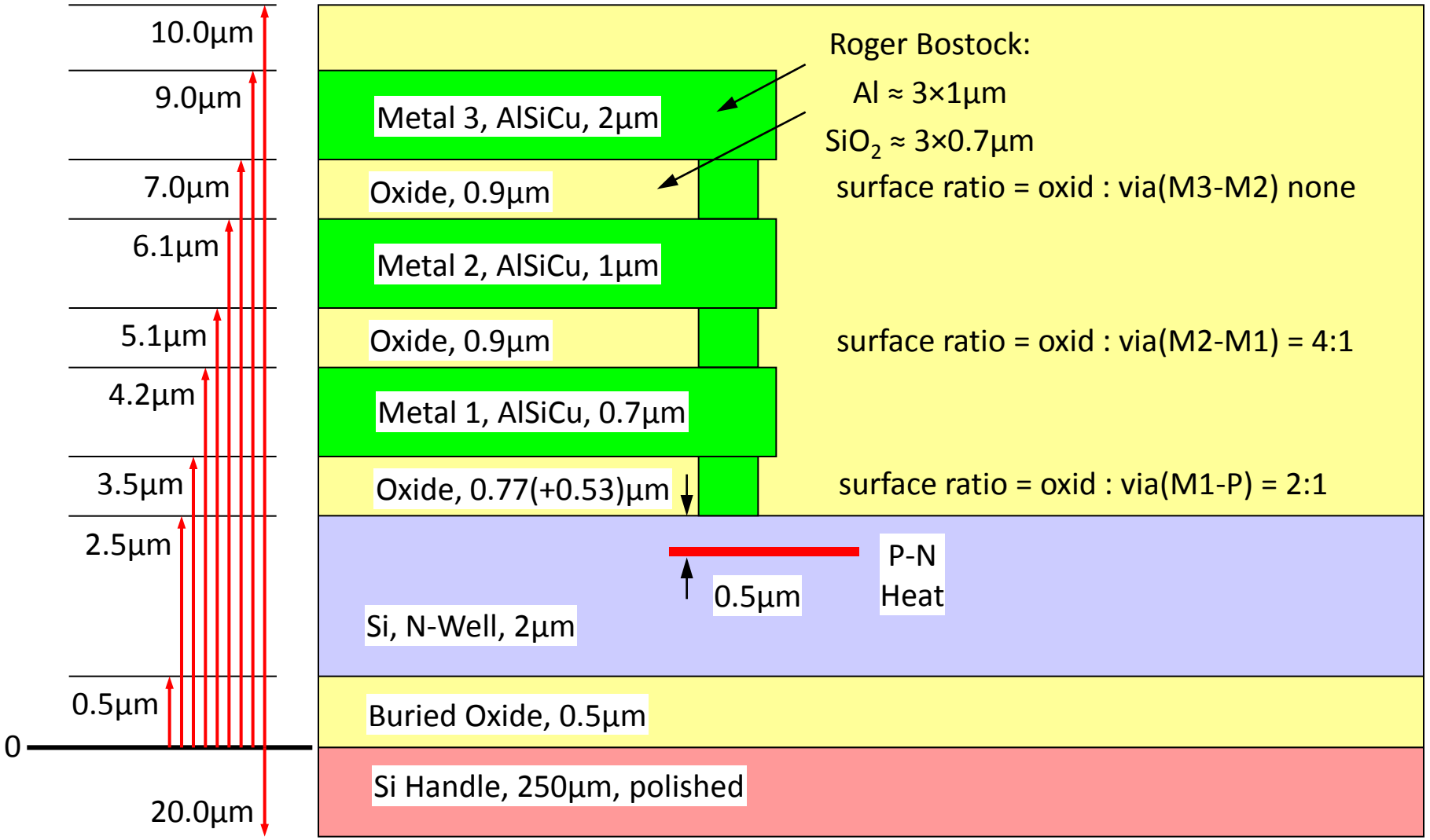
$$T_j(t) = T_{j1} - T_{j1} \cdot e^{-\left(\frac{t}{R_1 \cdot C_1}\right)} + T_{j2} - T_{j2} \cdot e^{-\left(\frac{t}{R_2 \cdot C_2}\right)} + T_A$$

Seal Ring



Confidential

Layer Thickness



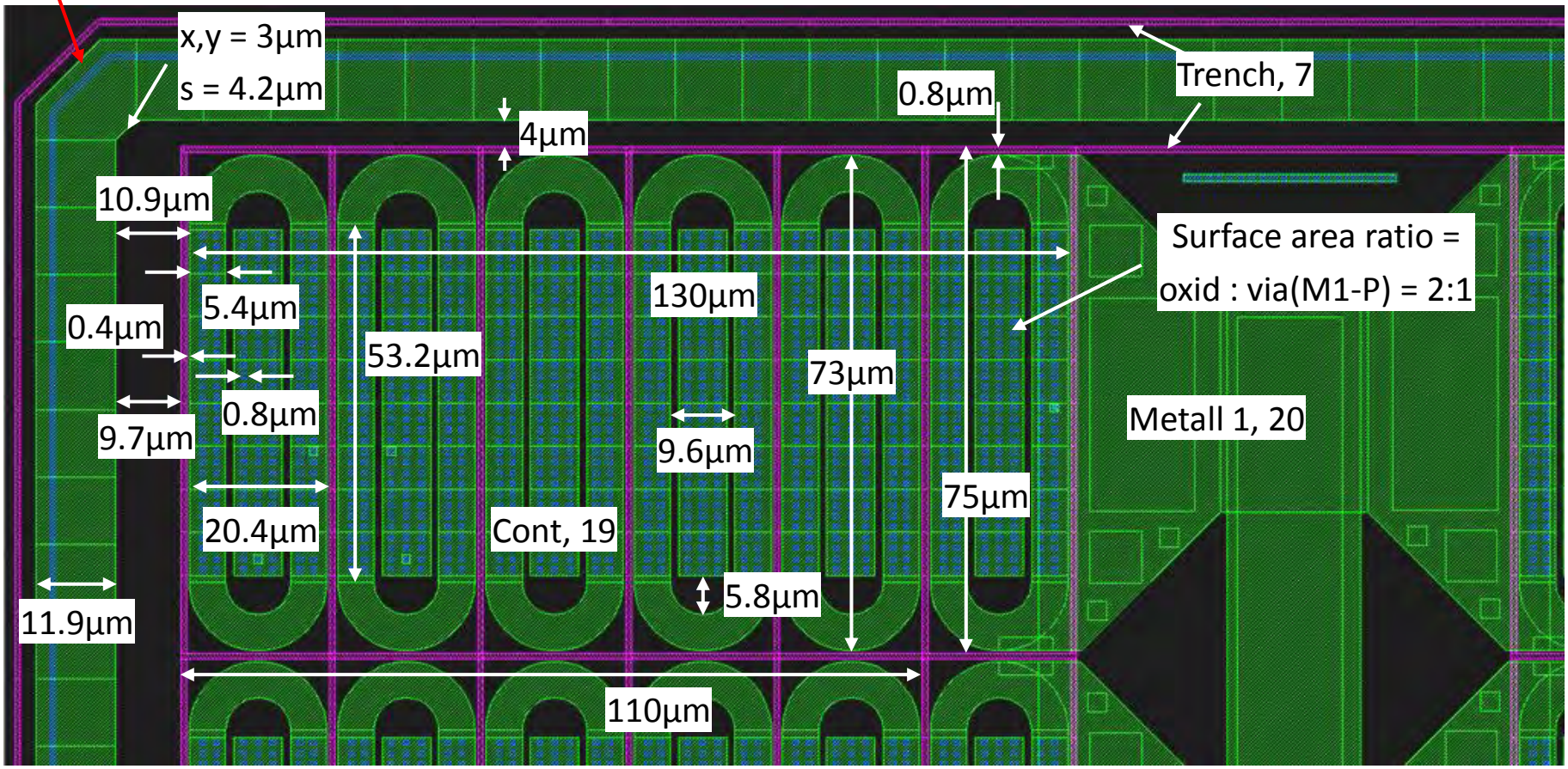
Dimensions

x,y = 9.6µm

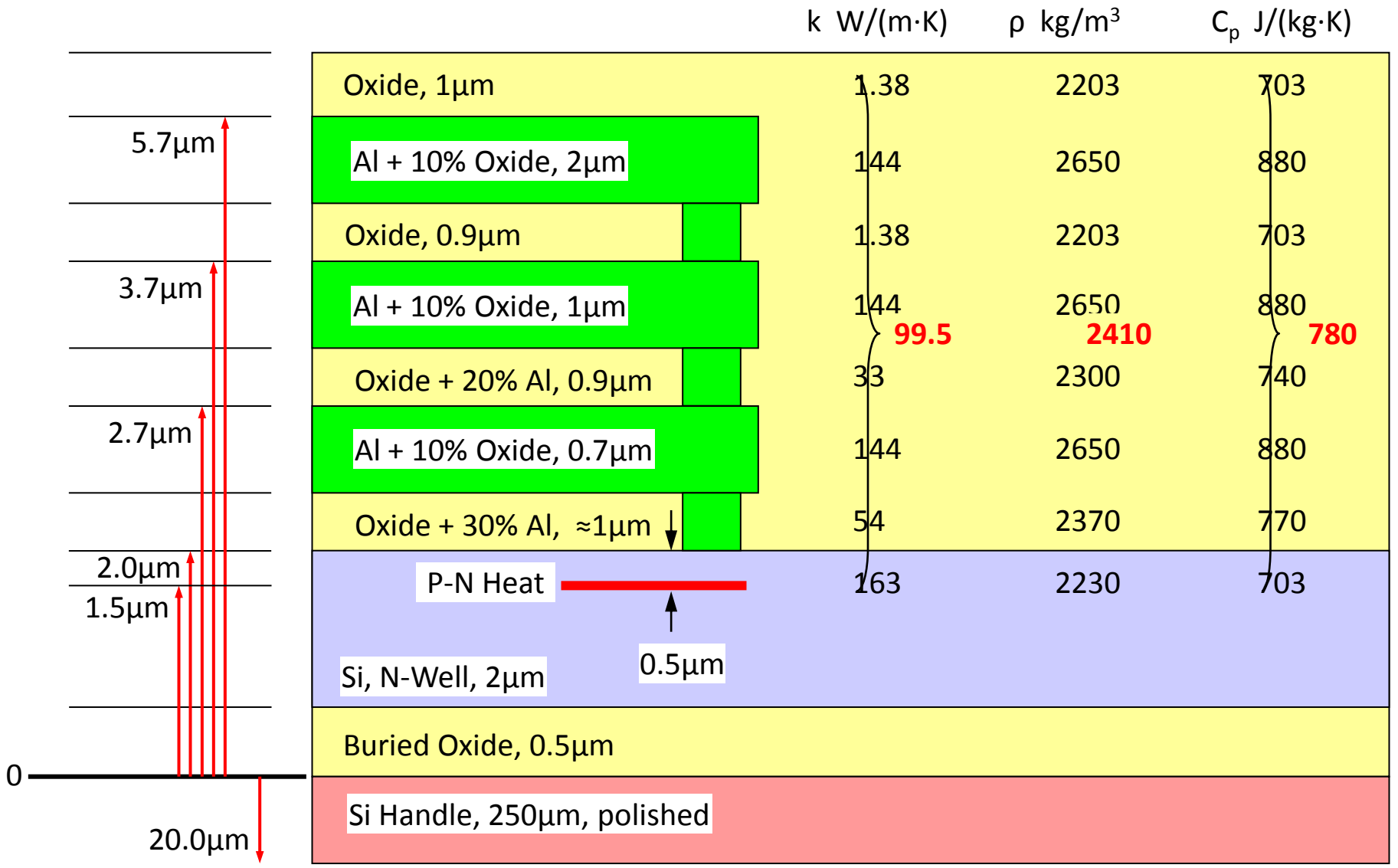
s = 13.6µm

Area ratio = oxid : via(M2-M1) = 4:1

Area ratio = oxid : via(M3-M2) = almost inexistent



Layer Model


k W/(m·K)
ρ kg/m³
Cp J/(kg·K)
Oxide, 1µm
1.38
2203
703
Al + 10% Oxide, 2µm
144
2650
880
Oxide, 0.9µm
1.38
2203
703
Al + 10% Oxide, 1µm
144
2650
880
99.5
2410
780
Oxide + 20% Al, 0.9µm
33
2300
740
Al + 10% Oxide, 0.7µm
144
2650
880
Oxide + 30% Al, ≈1µm
54
2370
770
P-N Heat
163
2230
703
0.5µm
Si, N-Well, 2µm
Buried Oxide, 0.5µm
Si Handle, 250µm, polished
5.7µm
3.7µm
2.7µm
2.0µm
1.5µm
0
20.0µm