Heat Removal of a Protection Chip after Surge Pulse

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Abstract: Sensors for industrial and automotive applications require electro-magnetic compatibility protection elements. It is an advantage to incorporate the protection elements directly in the application specific integrated circuit (ASIC). These protection elements however experience significant electrical stress and extensive heating on a short time-scale. It was therefore impossible to apply the conventional IC design process. We established new design rules. For this we first had to understand and quantify the device heating. To do so we used the finite element method (FEM) to model the surge pulse in a protection circuit of a test chip.
Owing to our results, the company HMT microelectronic AG at Bienne (Switzerland) was able to integrate high-voltage surge pulse protection elements directly in their ASIC designs. This innovation has met wide acclaim within the sensor industry. A decisive factor for this success was our thermal compact model which led to new IC design rules.

Keywords: Electro-magnetic compatibility (EMC), finite element modeling (FEM), high-voltage surge pulse, chip heating.

1. Introduction

Industrial sensors are connected with lengthy cables, typically measuring up to 20 m. The cables are in particular exposed to electro-magnetic fields from nearby power equipment, such as electrical motors and arc welders. The sensors must be electrically robust to cope with harsh environment.

The company HMT microelectronic AG at Bienne (Switzerland) develops integrated circuits (chips) for sensors in such industrial environment. HMT has recognized the advantage to integrate surge protection elements directly into the chip, giving small and cost-effective protection of the ICs. The small size and the large power dissipation however cause significant heating of the protection elements.

We analyzed the heat flux of the protection elements with the method of finite elements (FEM). A thermal characterization of test chips is presented in this paper.

2. FEM Model

Stationary and transient FEM computations were performed using the *Heat Transfer Module* of COMSOL Multiphysics®. The module solves the heat diffusion equation:

$$\rho c_p \frac{\partial T}{\partial t} - \nabla(k \nabla T) = Q$$

where ρ is the material density in kg/m^3, c_P is the specific heat at constant pressure in $J/(kg \cdot K)$ and k is the thermal conductivity in $W/(m \cdot K)$. T is the temperature field in K and Q is the heat source (positive) or heat sink (negative) in W/m^3. This equation has been solved analytically for various standard examples in classical text books, see e.g. [1] and [2].

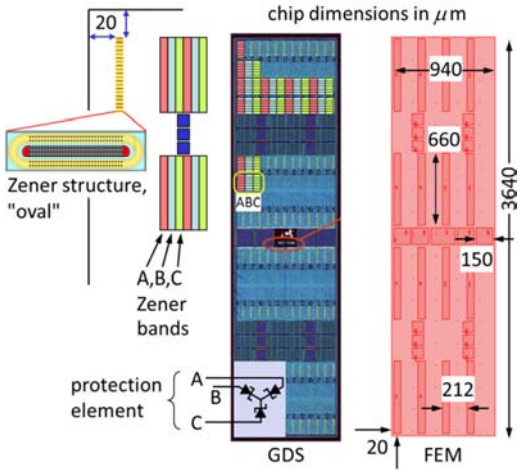

Figure 1. Chip layout of protection elements. The chip consists of Zener structures grouped to A, B, C "bands". Heat is dissipated underneath these bands. The FEM model to the right includes only A bands, which release 90% of the heat.

Figure 1 displays the protection test chip. 4×6 Zener structures ("ovals") are grouped to a "Zener band". The bands form the "Zener protection elements". Drawings and graphic data system (GDS) layout of the test chip are shown in the left and center part of figure 1. The FEM model and its dimensions are depicted on the right of the figure. Figure 2 shows details of the test chip. The chip has been fabricated with a silicon-on-insulator (SOI) technology.

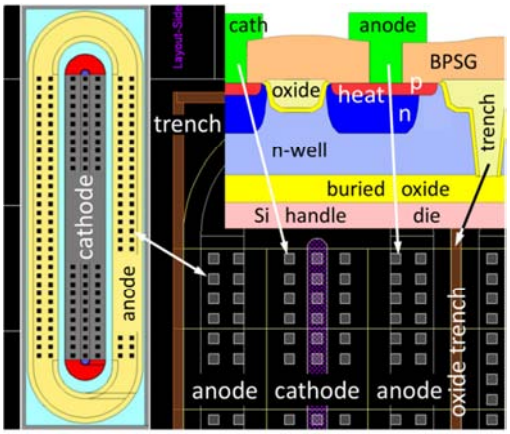

Figure 2. Details of the GDS layout compared to schematic drawings of the Zener structure (two insets, bright colors). The left inset displays a top view on the Zener structure with an oval ring-anode (yellow) and a cathode stripe (grey). The right inset shows a cross sectional drawing of the anode with the **p**-**n** junction, where heat is released. BPSG stands for boron-phosphorus-silicate-glass. The buried oxide and the oxide trenches cause efficient thermal insulation (see text).

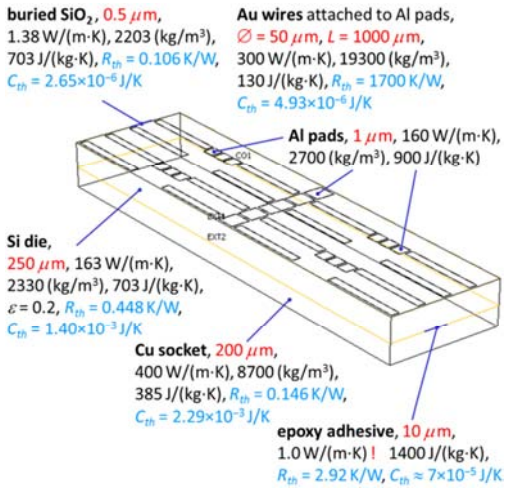

Figure 3. Model data such as thickness and material parameters used for simulation and consistency checks. A presumed diameter ∅ and length *L* of gold wires are also indicated. The data can be used to calculate the thermal resistance and the heat capacitance of every part of the model.

The relevant data of the FEM model at 20°C are summarized in figure 3. The (layer) thickness of parts of the die is indicated. An assumed diameter ∅ and length *L* of gold bond-wires are also specified. The values for the thermal conductivity *k*, the material density ρ and the specific heat c_P are listed in the figure. The dimensions together with the material parameters yield the thermal resistance R_{th} and heat capacitance C_{th} of different parts of the test chip. These *R*-*C*-values are used for estimations of time constants and maximum temperatures reached in a stationary situation (see below).

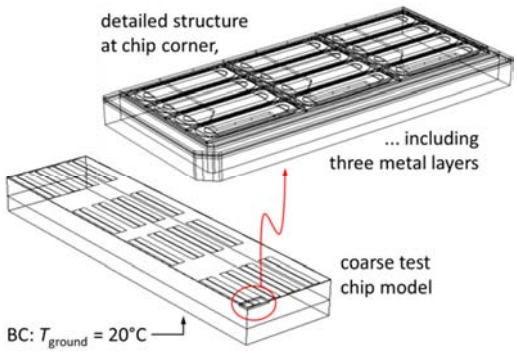

Figure 4. Detailed and coarse FEM model of the test chip. The bottom of an assumed copper socket is the thermal ground held at 20°C. The coarse model contains A and B Zener bands, which release 90% and 10% of the heat, respectively.

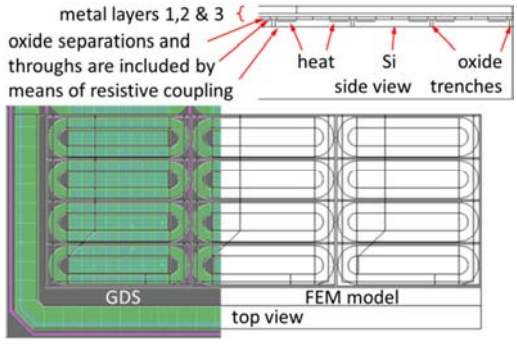

Figure 5. The top part of the figure displays a cross sectional view of the detailed FEM model. GDS layout (colored) and the detailed FEM model (top view) are compared at the bottom of the figure. The semiconductor and metal and oxide layers are accurately reproduced in the FEM model.

The final FEM study was performed with a detailed model of the layer structure at the chip corner, the hottest sector of the die. The detailed model is embedded in a coarse model (see figure 4). The detailed model contains "oxide boxes" which are a key feature to understand the very fast temperature rise in the active silicon layer. The explicit structure of the chip layers is precisely reproduced in the detailed FEM model of figure 5.

The die was assumed to be attached with epoxy adhesive to a copper socket. We used the following boundary conditions. The bottom of the copper socket was defined as thermal ground at fixed 20°C (see figure 4). The top of

the chip consisted of uniformly distributed, heated "Zener bands" which dissipate together 253 W. The epoxy adhesive between the silicon die and the copper socket emulates the quality of thermal anchoring to the ground at 20°C.

The automotive surge pulse ISO 7637-2 dissipates the most heat of all studied standards. We chose it as the benchmark pulse for our investigations. Figure 6 displays its heating power as a function of time. The pulse generates a maximum power of 253 W.

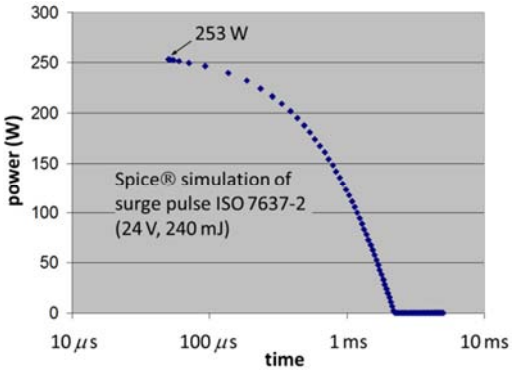

Figure 6. Heat generation as a function of time for surge pulse ISO 7637-2. The Spice circuit analysis yields a peak power of 253 W.

3. Stationary Study of Coarse Model

The objective of the stationary computation was to understand the heat flux. We analyzed the role of the die attach, the surface radiation, the possible bond wires, the seal ring and of the conduction to ambient air.

253 W simulated Joule-heating in the active silicon layer of our test chip yields a (impractical) maximum steady state temperature of 1116°C, see figure 7A. Note however that the real protection elements are never exposed to such stationary conditions. The conductive and radiative heat loss to ambient air is computed by means of the equations:

$$P_{air} = h \cdot A\left(T_{surf} - T_{amb}\right)$$

$$P_{rad} = \varepsilon \cdot \sigma_B A\left(T_{surf}{}^4 - T_{amb}{}^4\right)$$

where P is the power in W, h is the heat transfer coefficient in W/(m^2·K), A is the chip surface in m^2 and T is the temperature in K of the chip surface and the ambient air, respectively. ε is the surface emissivity and σ_B the Boltzmann constant. Due to the very small chip surface A of about 5.5×10^{-6} m^2, counting also the side walls, the heat removal to ambient air is negligible for both, convection/conduction and radiation. This can be observed in figure 7B. Figures 7C and D display computations including gold bond-wires and a seal ring as a *highly conductive layer*. We conclude that the maximum temperature of the chip is governed by the contact resistance between die and socket, i.e. the resistance of the epoxy adhesive. This is demonstrated in Fig. 8. The thickness of the epoxy and thus its resistance are reduced by a factor 10 in figure 8B. This measure lowers the maximum temperature drastically. Most desirable therefore is well conducting and thin epoxy adhesive. For instance Epo-Tek H20E [3] exhibits a thermal conductivity k of 29 W/(m·K) and an electrical resistivity of 4×10^{-6} Ωm.

The above simulations and considerations suggest that the heat removal can be represented in a simple 1-dimensional series of thermal resistances. Figure 9 shows a compact model consisting of 4 thermal resistances: the buried silicon oxide, the silicon die, the epoxy adhesive (k = 1 W/(m·K)) and the copper socket (compare to figure 3). An input power of 253 W multiplied with the overall thermal resistance of 3.63 K/W yields a stationary temperature increase of 920 K. This estimation compares to the FEM computations of figure 7, where the chip surface temperatures vary between 800°C and 1100°C. The heat capacitance of the silicon die and the copper socket complete the thermal circuit of figure 9.

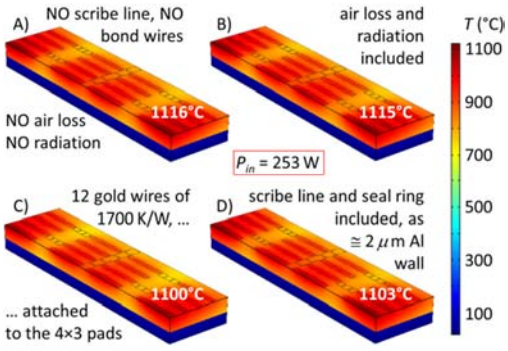

Figure 7. Steady state surface temperature of the test chip exposed to 253 W continuous power input. The power is dissipated underneath the 16 "Zener bands". Various heat channels are considered (see text). The values of the different images denote the maximum temperatures reached on the surface, near the corner of the chip.

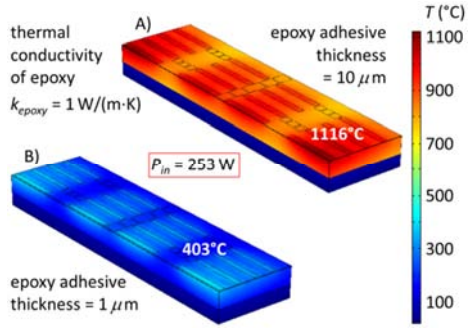

Figure 8. Steady state surface temperature of the test chip subjected to 253 W. The difference between plot A) and B) is the epoxy resistance. A 10 times smaller epoxy resistance reduces the surface temperature considerably. Values in the pictures indicate maximum temperatures.

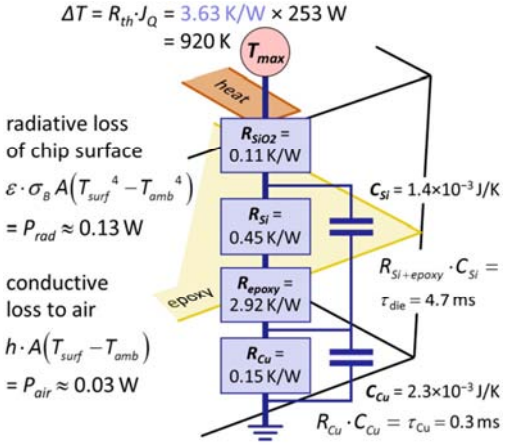

Figure 9. Ab initio compact model of the test chip. 4 thermal resistances are connected in series to the thermal ground. The heat source (chip surface) attains the maximum temperature in steady state conditions. The heat capacitance of the silicon die and of the copper socket are added to the thermal circuit. Two time constants τ_{die} = 4.7 ms and τ_{Cu} = 0.3 ms can then be calculated.

To investigate the specific temperature evolution of the Zener structures themselves, a transient study of a detailed model was necessary.

4. Transient Study of Detailed Model

We performed transient thermal simulations with the detailed model of the figures 4 and 5 to determine the precise time constants of the protection elements.

Figure 10 displays the distribution, the area and the power of the heat sources ("anode stripes") in the COMSOL geometry. Two examination points PT1 and PT2 are shown in Fig. 10, where the temperature evolution is recorded after a heat step. The heat step rises within 10 ns and is displayed as an orange line in figure 11. The temperature of both test points rises in two legs. The two legs can be understood as two first order low pass filters with time constants given by a resistance and a capacitance in parallel. The first rise to about 300°C can be attributed to the heat flux in the active silicon layer, above the buried oxide. The second temperature increase represents the heat flux through the silicon handle and the copper socket. Its time constant is of the order of milliseconds, as expected from the thermal *R-C* circuit (see figure 9). The initial temperature rise is steeper in the detailed model (PT1, blue curve) compared to the coarse model. The initial heat dissipation in the detailed model is limited to the "Zener oxide boxes" which are composed of the buried oxide layer and the oxide trenches. The heat is smeared out to the surface in the coarse model, where no trenches hinder horizontal heat flux. An oxide box represents a highly efficient thermal barrier in all directions. Therefore a heat source within an oxide box increases the local temperature faster than in the coarse model. After about 100 µs the further temperature rise of both test points is synchronous.

Figure 12 reveals the extremely fast temperature rise within the oxide box after the first few microseconds. The initial slope of PT1 corresponds to a heating rate of 60 K/µs.

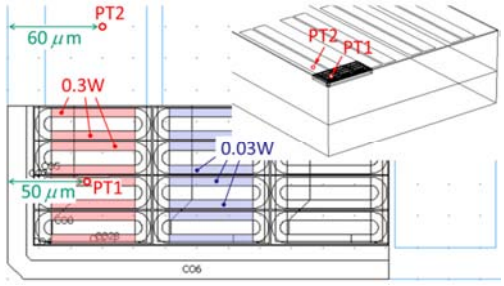

Figure 10. Top view of detailed COMSOL model. The power input of 253 W is distributed to A (red) and B (blue) stripes of the Zener anodes (compare to figures 1, 2 & 5). 0.9×253 W /16 /(4×6×2) = 0.3 W are dissipated in every A stripe. Top right is a 3D-perspective representation of the detailed model, embedded in the corner of the die. Two test points PT1 and PT2 are used to plot the temperature evolution. The dimensions give the distance of the test points to the chip edge.

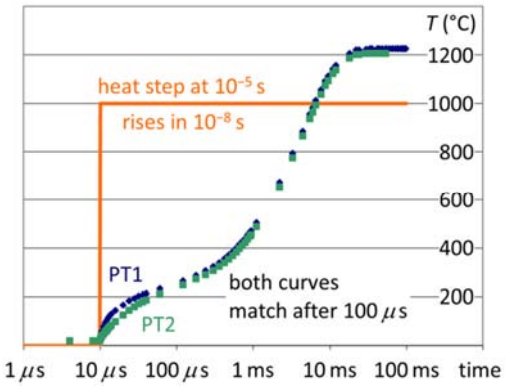

Figure 11. Simulated temperature evolution at test points PT1 and PT2 after a heat step. The test points are in the active silicon structure of both, the detailed and coarse model. Note that the heat sources here are slightly different than in figure 7 !

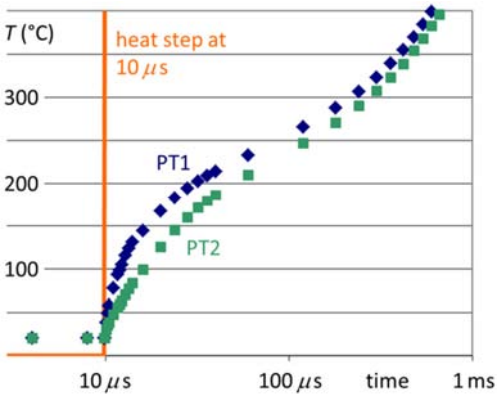

Figure 12. Initial temperature evolution at test points PT1 and PT2 after heat step. The temperature of PT1 rises by about 60 kelvin per microsecond !

5. Measurements of Test Chip

The thermal simulations could be validated by measurements. An aluminum resistance was integrated in the test chip inside the protection elements. The resistance was calibrated to be used as a temperature sensor. Ultra-fast temperature measurements are displayed in figure 13. Note the excessively high junction temperature of 153°C after mere $20\,\mu s$.

The definite performance of the protection elements is characterized by voltage-current (V-I) graphs. The very small, local thermal time constant complicates accurate V-I measurements at steady temperature. As a consequence we built our own pulse generator for ultra-short-300 ns 10 A - 70 V signals to establish the V-I characteristics of the protection elements.

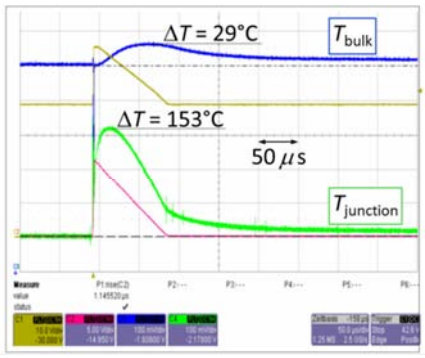

Figure 13. Measured temperature evolution of the bulk silicon and the junction during a 2.0 A surge impulse-equivalent (triangular shape). Time axis is $50\,\mu s$ / div. The signal was produced with an adequate pulse generator (see text).

6. Compact Model

The ab initio compact model of figure 9 reproduces qualitatively the simulated temperature evolution of the junction (PT1 & PT2 of figure 11). However the initial temperature rise (not shown) of the ab initio compact model is far too faint and the final temperature too low. The notion of a 1D vertical heat flux through the whole cross sectional area of the chip is simply not correct, as discussed above.

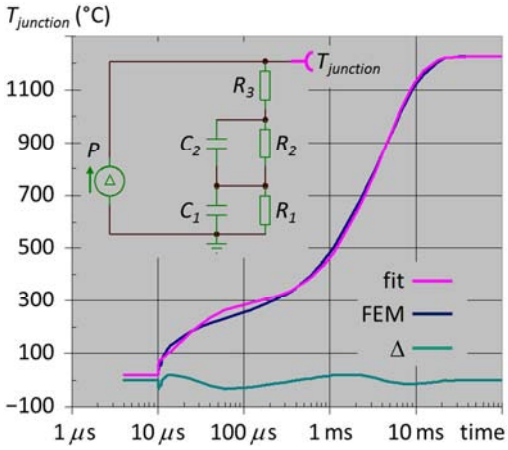

Figure 14. Four-parameter fit of the junction temperature. The blue curve denotes the FEM simulation, i.e. PT1 of figures 11 & 12. The pink curve is an exponential fit (see text). Green represents the difference between the two curves. The inset shows the compact model to calculate the temperature evolution of the junction.

A more adequate electrical-equivalent lumped model is presented in figure 14. The four quantities R_1, C_1, R_2 and C_2 are not calculated from geometry and material data as

in figure 9, but are fit parameters to the equation for the temperature as an exponential function of time:

$$T_J(t) = T_G + T_1\left(1 - e^{\frac{-t}{R_1 \cdot C_1}}\right) + T_2\left(1 - e^{\frac{-t}{R_2 \cdot C_2}}\right) + T_3$$

where T_J is the junction temperature, T_G is the thermal ground at 20°C and t is the time. The parameters must satisfy the following constraints:

$$T_J(t{=}\infty) = 1225°C \text{ (FEM)}$$

$$T_1 = P \cdot R_1 \quad T_2 = P \cdot R_2 \quad T_3 = P \cdot R_3$$

$$R_{tot} = R_1 + R_2 + R_3 = \frac{T_1 + T_2 + T_3}{P}$$

Table 1: Parameters for the compact model of figure 14. The values in the green boxes were obtained by a least square fit of the equation above to the FEM curve (PT1) of figure 11. Note, R_3 is not a fit parameter but a result of the constraints.

Parameter	Value	Unit
P	253	W
$T_J = T_G + T_1 + T_2 + T_3$	1225 ✓	°C
T_3	48	K
R_3 "oxide trench"	0.19	K/W
T_2	199	K
$\tau_2 = R_2 \cdot C_2$	1.8×10^{-5}	s
C_2 (fit) "active silicon"	2.3×10^{-5}	J/K
R_2 (fit) "buried oxide"	0.79	K/W
T_1	958	K
$\tau_1 = R_1 \cdot C_1$	4.2×10^{-3}	s
C_1 (fit) "die + epoxy"	1.1×10^{-3}	J/K
R_1 (fit) "die + epoxy"	3.79	K/W

The least square fit yields the parameters in the green boxes of table 1. The presumed origin of the five model parameters R_1, C_1, R_2, C_2 and R_3 is given between quotation marks in table 1. Inspection of figure 14, in particular the difference Δ between the curves evidences the good quality of the fit. The resistance $R_{top} = R_2 + R_3 = 0.98$ K/W is almost an order of magnitude larger than that obtained by 1D-ab initio calculations (compare to figure 9). The larger R_{top} value corresponds to a smaller active Zener area. The fitted heat capacitance $C_2 = 2.3\times10^{-5}$ K/W is about three times smaller than the ab initio 1D-value. Expected was a factor 5 by simple comparison between the volumes of the oxide boxes and the top layer.

There are still more fitting possibilities and the procedure could be improved. The mechanism of the heat flux, however, is essentially understood: It is a channeled flux by the oxide trenches in the active top layer and it is a 1-dimensional heat flux in the silicon handle.

7. Conclusions

The heating of surge pulse protection elements was modeled by means of the finite element method. Stationary and transient simulations of a test chip established the following results:

1. The maximum temperature is governed by the die attach to the base, i.e. by the conductivity and the thickness of the epoxy adhesive.
2. Heat flux through bond-wires or by conduction or radiation to air is negligible.
3. Oxide trenches in the active silicon layer and the buried oxide cause efficient thermal insulation.
4. The initial temperature rise after a heat step emulating surge pulse ISO 7637-2 is incredibly fast: The junction temperature increases by 60 K/μs.
5. A compact model based on exponential fitting reproduces the temperature evolution of the FEM simulation accurately.
6. We were able to measure the initial temperature increase and confirm the simulations and the compact model.

The mechanism of heat flux and temperature evolution of the test chip is principally understood. Material and geometry data of similar chips allow for prediction of the temperature evolution prior to FEM simulations.

Owing to our results and compact model, the company HMT could successfully integrate high-voltage surge pulse protection elements directly in their ASIC designs. The elements can absorb 2 A/40 V impulses at ambient temperatures up to 200°C. To our knowledge no competitor has been able to reproduce such robust and user-friendly EMC-protections.

8. References

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3. Polytec PT GmbH, 76337 Waldbronn, Germanny

9. Acknowledgements

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