High Curvature Bending of Ultra-thin Chips and Chip-on-Foil Assemblies

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Abstract: Ultra-thin chips of less than 20µm become flexible, allowing integration of silicon IC technology with highly flexible electronics. During use the ultra-thin chips in these products can be bent to a very high curvature, sometimes to less than 1mm bending radius, putting a large strain on the chips. In this paper the stress distribution in ultra-thin chips at very high curvatures is evaluated, using a modified four-point bending method. The structural mechanics module in COMSOL is used including contact modelling with friction. Results including the deformation and stress distribution in the chip are evaluated for different curvature levels during the test. Contact and frictional effects at the chip-support interface at high deformation ('push through' effect) are discussed. The effect of chip thickness and geometry is investigated. The modelled stress distributions were compared to failures observed in experimentally tested thin chips.

Keywords: Structural mechanics, contact modeling, friction modeling, four point bending.

1. Introduction

Ultra-thin chips of less than 20µm become flexible, allowing integration of silicon IC technology with highly flexible electronics. This combination allows for highly intelligent products that are thin, flexible and low-cost [1, 2]. Examples include sensor systems integrated into food packaging or healthcare and sport monitoring tags integrated in clothing textile or even as wearable patches directly on the skin (see figure 1). A high level of intelligence and communicative capabilities are can be added to these devices by integrating chips and thin passives directly on the foil itself. To preserve low thickness and therefore flexibility of these systems, thinned bare die chips, thin passives and unpackaged LEDs are used. During use the ultra-thin chips in these products can be bent to a very high curvature, sometimes to less than 1mm bending radius, which puts a large strain on the

Figure 1. Ultra-thin chip bent between fingers (top left), Flexible monitoring tag (top right) 3 and skin temperature sensor patch (bottom).

chips. It is imperative to understand the stress distribution in the chips and to optimize the chip design (for instance: thickness, layers and bondpad/bump locations) or the assembly design (such as foil thickness, conducting track properties and layout, encapsulation/underfill).

The bending stresses that are developed in the chip at a certain bending radius can be simulated by modeling a 4-point bending test. The 4 point bending test consists of applying a load on the test specimen using 4 struts, two inner struts on one side and two outer struts on the other side of the specimen. The model is depicted in figure 2. The chip in this figure has dimensions 2.4 x 2.4 x 0.02 mm^3. The model in figure 2 contains 4 circular metallic (Ni) bumps corresponding to typical bonding pads on the silicon chip. Bare silicon dies without bumps were also modeled for verification with experiments (see section 4). The four point bending setup dimensions are inner strut spacing of 0.9 mm, an outer strut spacing of 1.7 mm and strut diameter of 0.2 mm.
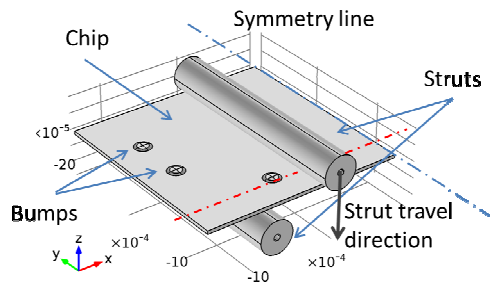
Figure 2. Four-point bending model. For symmetry reasons ¼ of the structure is modeled. The black arrow points in the direction of the strut travel. The bottom strut is fixed. The red cut-line runs along the bottom of the chip under the middle of the bumps.

2. Use of COMSOL Multiphysics

The material model used will follow the stress-strain relations in the material using the second Piola-Kirchhoff stress tensor and the Green-Lagrange strain tensor. Time dependent modeling is used, to allow visualization of the sliding friction at different stages, though a quasi-static implementation suffices since deformation rate is low. The governing equation for the linear elastic material model is:

$$-\nabla \sigma = F_V$$

where $\sigma = S$ and F_V is the volumetric force vector. The linear elastic material model is used, including geometric non-linearity, because large deformations are present in the structure and sliding friction is encountered. The geometry contains thin components which deform out-of-plane, leading to large deformations, though strains remain moderate thus the linear-elastic model remains valid, especially for the brittle silicon material that is used. The stress-strain relationship is as follows:

$$s = s^0 + C : \left(\varepsilon - \alpha\theta\, \mathbf{I} - \varepsilon^0 - \varepsilon^i \right),$$

where S^0 and ε^0 are the initial stresses and strains in the material, α is the thermal expansion matrix, with $\theta = T - T_{ref}$, and ε^i represents the inelastic strains. C is the elasticity matrix.

The total strain tensor, ε, as a function of volumetric displacement, $\mathbf{u}$, is:

$$\varepsilon = \frac{1}{2}\left(\nabla\mathbf{u} + \nabla\mathbf{u}^T \right)$$

Contact modeling is employed for the contacts between the support struts and chip surface. The contact model is defined by calculating the penalized contact pressure, T_{np}, as a function of the gap distance, d_g:

$$T_{np} = \begin{cases} T_n - p_n d_g & if \quad d_g \leq 0 \\ T_n e^{\frac{p_n d_g}{T_n}} & otherwise \end{cases}$$

where p_n is the normal penalty factor. Initially, the support struts are situated 1 µm apart from the chip surface at the start of the simulation. The chip is deformed by the applied displacement of the top strut (see figure 2) when it comes into contact with the chip. The bottom strut is fixed to catching

A sufficiently low initial time step must be applied, to avoid missing the contact surfaces between the struts and (floating) chip.

3. Experimental

A four point bending setup for ultra-thin chips is presented in Figure 3. It consists of a custom made 4 point bending insert mounted on a microscope tensile stage (Linkam TST350). The chip is placed between the upper and lower loading struts (green line in Figure 3). Exact parallelism between the inner and outer struts is realized in the design by 5 DOF adjustable struts and a mechanical alignment mechanism. Details of this method are given in reference [4].
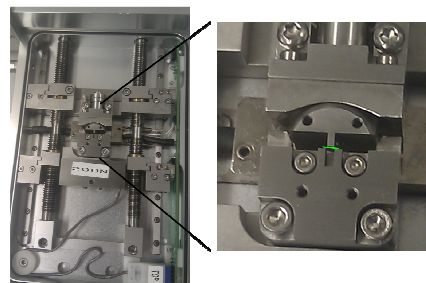
Figure 3. Bending setup for thin chips.

4. Model verification

The modeling results were compared to experimental results for a bare silicon die (no bumps). The results of the model verification are presented in figure 4.
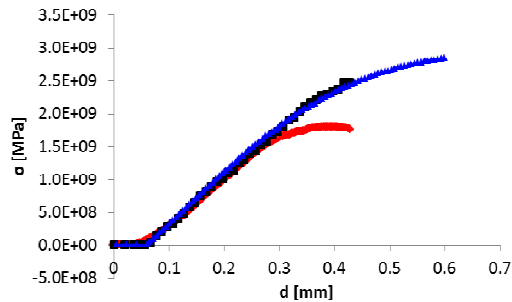

Figure 4: Tensile stress (σ_{xx}) in the chip as a function of support strut travel. The strength of the thin chip calculated using the COMSOL model is compared to the stress calculated using the radius monitoring method (black) and to the predicted strength using conventional 4 point bending formula (red).

In figure 4, a comparison is made between the stress as determined by COMSOL model, the stress determined by the radius monitoring method and the stress determined by conventional 4 point bending formula. The tensile stress in the outer edge across the middle of the die in the COMSOL model is taken (i.e. in the x-z symmetry plane at y = 0 and z = 10 µm). The stress in the die as calculated using the standard 4 point beam bending formula is shown to be inaccurate for the high curvature of the thin dies. The tensile stress in the outer edge of the die is underestimated due to the large deformation and sliding of the die at the supports. The stresses determined using the COMSOL model correlate well with the radius monitoring method results up to die failure. The radius of the die is not affected by sliding at the supports (the so called 'push through' effect), whereas the conventional 4-point bending method underestimates the maximum dies stress by up to 50% in the example in figure 4.

5. Results and discussion

In figure 5 the stress distribution in xx-direction (S_{xx}) in the bumped die is presented. The bottom of the die is subjected to tensile stress. The influence of the bumps is clearly visible at the bottom of the die. The maximum stress in the die occurs adjacent the bump locations and is around 2.2 GPa. This peak is also visible in figure 7, though the data in figure 7 is taken at a lower strut travel of 0.12 mm for the 20 µm thick die.
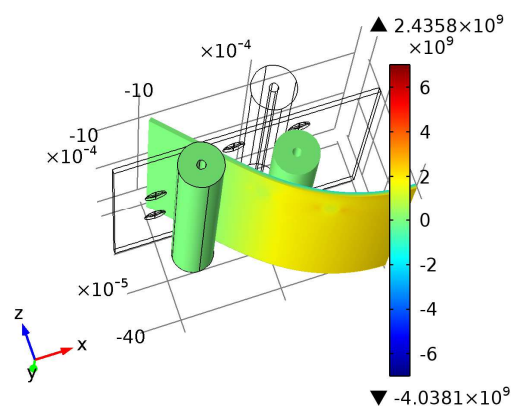
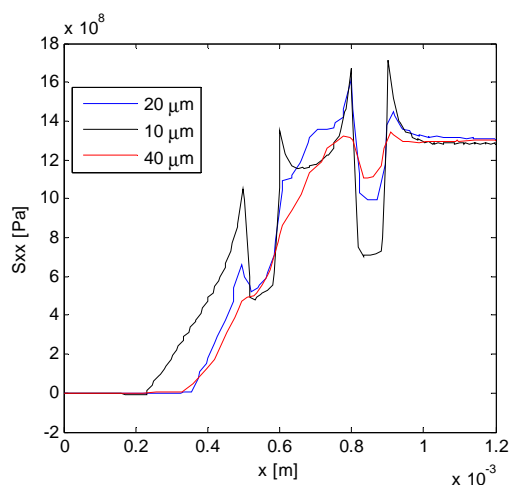**Figure 5**: Second Piola-Kirchhoff stress distribution in xx-direction (S_{xx}) in the bumped die at 0.3 mm strut travel for a 20 µm thick die.

In figure 6 the influence of thickness of the die is presented. For 10 µm thick dies the stress in the die is considerably lower, around 1.3 GPa, while the maximum stress for the 40 µm thick die is around 4.8 GPa at 0.3mm strut travel. The thickness of the die is of influence on the maximum stress at the outer edge of the die for a given curvature, which corresponds to a certain strut travel. However, the influence of the bumps seems to decrease with chip thickness. This effect is also visualized in the figures 7 and 8. In figure 7 the stresses around the bump locations are visible. The stress distribution is shown along the cut line indicated by the red line in figure 2
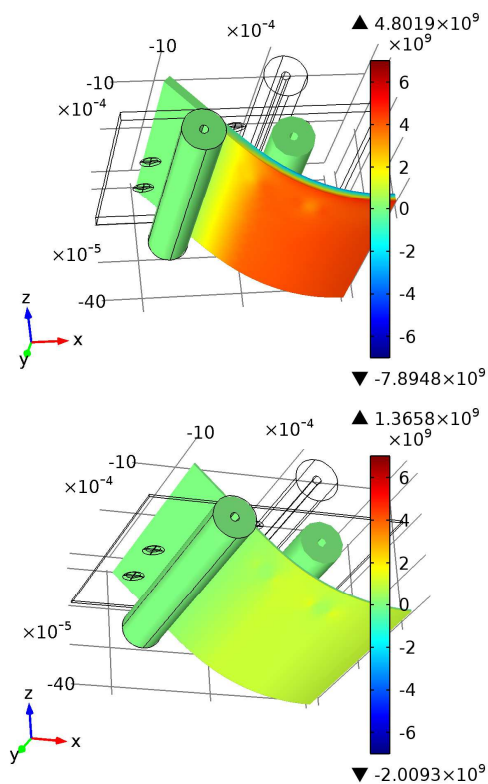
Figure 6: Second Piola-Kirchhoff stress distribution in xx-direction (S_{xx}) as in the bumped die at 0.3 mm strut travel for 40 µm thick die (top) and a 10 µm thick die (bottom).


Figure 7: Second Piola-Kirchhoff stress distribution in xx-direction (S_{xx}) in bumped dies with different die thickness along the cut line indicated in red in figure 2.

In figure 7 the influence of Nickel bumps with a fixed height of 6 µm on the back side stress distribution is presented. The strut travel displacement is different in each 3 cases and chosen in such a way that the stresses are equal in the middle of the die (i.e. at the intersection of the cut-line and the symmetry axis at x = 1.2 mm). In figure 7, the magnitude of S_{xx} starts to increase at different locations along the x-axis of the die. This is the result of the frictional effects at the outer support strut, where sliding occurs. The difference in stress distribution between the samples around x = 0.7 mm is also result of the sliding of the chip along the top support strut. In figure 8 the influence of bump height on the stress distribution at high curvature (at 0.4 mm strut travel displacement) is presented. Here, the stress between the inner support struts is not constant, but can be seen to increase towards the middle of the die (at x = 1.2 mm). However, the influence of the bumps still leads to a stress peak at the edge of the bumps for Nickel bumps higher than 1 µm, as can be seen in figure 9.
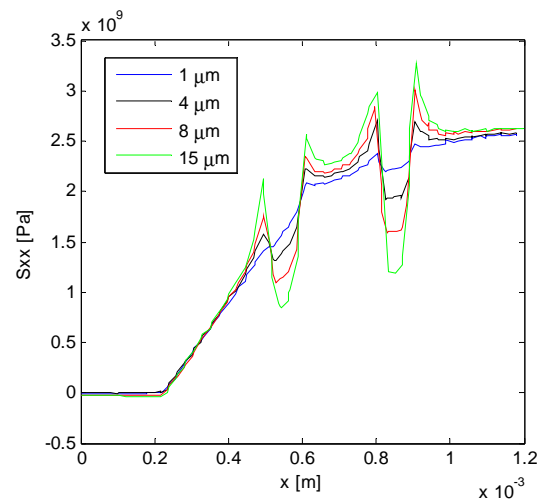

Figure 8: The influence of bump height on the stress distribution around the bumps (cut line position as indicated by the red line in figure 2).
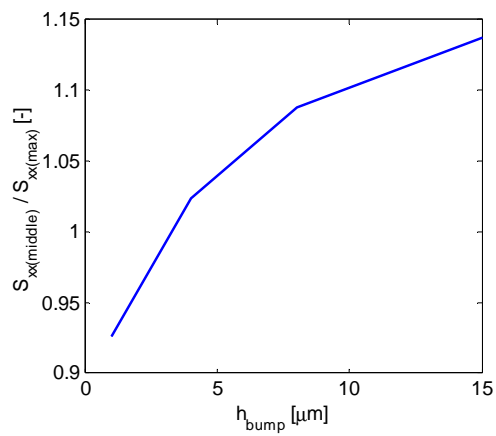
Figure 9: Ratio of peak stress adjacent to the inner bump ($S_{xx(max)}$) and the stress at the middle of the die at x = 1.2 mm ($S_{xx(middle)}$).

In typical failed chips (see figure 10) the crack line is often located close to the bump locations, i.e. corresponding to the position of the tensile stress peaks (as visualized in figures 7 and 8). Thus it is clear that for optimization of the bending strength of these thin chips it is imperative to control the bump height in comparison to the chip thickness.
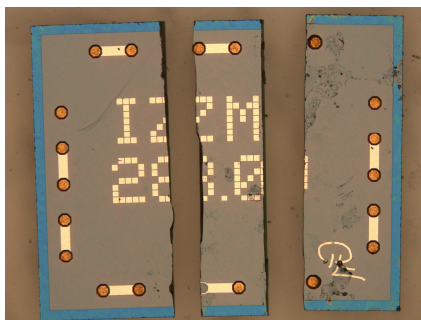

Figure 10: Example of a failed IZM28 chip after being subjected to bending stress. Image of the front side of the chip (i.e. the non-ground side).

6. Chip on foil assemblies

For devices as in figure 1, chip-on-foil assemblies are needed. These can be achieved by direct flip-chip bonding on flexible foils. A typical assembly is modeled in figure 12. Upon applying a bending moment stresses mainly develop inside the chip, which is the most vulnerable part in the assembly (figure 13). It was found that the stresses inside the chip can increase significantly for a chip-on-foil assembly compared to a stand-alone chip in the 4 point bending setup. Using the 4 point bending model it is possible to adapt the buildup of the stack in such a way that the stresses in the chip are minimized during bending. This will be the topic of future work.
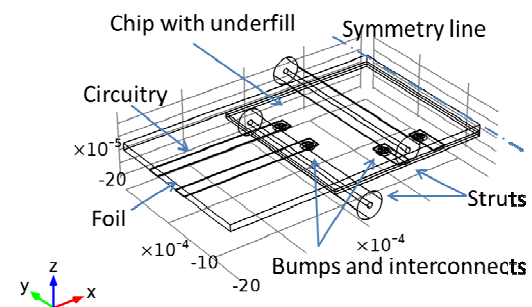
Figure 12: Model for a chip-on-foil assembly including chip, foil and conductive tracks. For symmetry reasons only ¼ of the geometry is modeled.
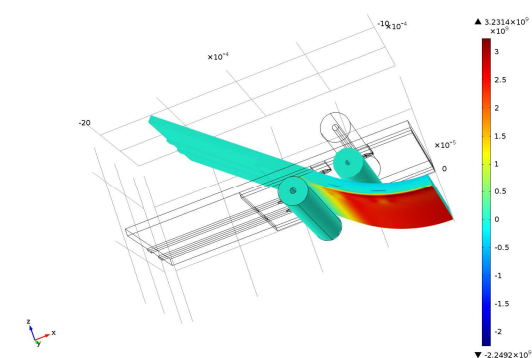
Figure 13: Second Piola-Kirchhoff stresses in x-direction (S_{xx}) inside the chip-on-foil assembly of figure 12.

7. Conclusions

A COMSOL model for 4 point bending of thin chips was developed, using linear elastic modeling with geometric non-linearity. The geometry contains thin components which deform out-of-plain, leading to large deformations. However, due to the limited thickness strains remain moderate thus the linear-elastic model remains valid The stress in the die as calculated using the standard 4 point beam bending formula is shown to be inaccurate for the high curvature of the thin dies. The tensile stress in the outer edge of the die is underestimated due to the large deformation and sliding of the die at the supports. The stresses determined using the COMSOL model correlate well with the radius monitoring method results up until die failure. For optimization of the curvature, thickness must be low, but in order to achieve a high bending strength for these thin chips the bump height must be limited in comparison to the chip thickness. It was found that the stresses inside the chip can increase significantly for a chip-on-foil assembly compared to a stand-alone chip in the 4 point bending setup. Using the 4 point bending model it is possible to adapt the buildup of the stack in such a way that the stresses in the chip are minimized during bending.

8. References

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9. Acknowledgements